RD50-MPW3:
A fully monolithic digital CMOS sensor for future tracking detectors

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on behalf of the RD50 CMOS collaboration

Aims and Environment

Goals RD50-CMOS
- Study and develop radiation hard semiconductor tracking sensors
- Depleted Monolithic Active Pixel Sensor (DMAPS)
- Fabricated in commercial CMOS process for low cost and high availability

RD50-MPW3: Possible applications
- Radiation environment: > $3 \cdot 10^{16}$ n_{eq}/cm^2
- collider experiments beyond LHC, e.g. FCC
- Fast tracker for medical imaging

Novelties RD50-MPW3
- Very small pixel (thus: high granularity) with analog + digital electronics inside for signal pre-processing and configuration of single pixels
- Digital readout using a single 640 MHz differential line
- Capability for synchronizing internal timestamp with other detectors

Key Facts

Fabrication
- LF15A process from LFoundry (150 nm)

High-resistivity wafers: 1.9 kOhm·cm, 3 kOhm·cm (nominal)
- Submitted to foundry: Dec. 2021, received: Aug 2022

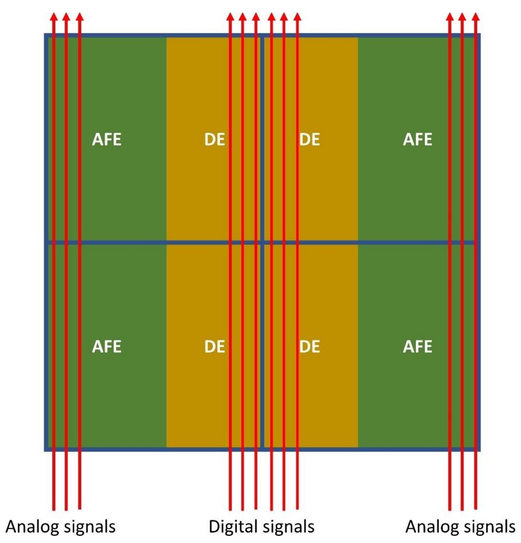
Layout
- Matrix of 64 x 64 pixels, pixel size: 6 2um x 62 um
- Digital periphery next to matrix, total chip size: 5.1 mm x 6.6 mm

Design
- FEI3-style pixel design based on predecessors RD50-MPW1 and RD50-MPW2
- Large collection electrode using deep N-well layer
- Analog-on-Top flow for chip level implementation

Testing
- Initial evaluation ongoing and successful so far

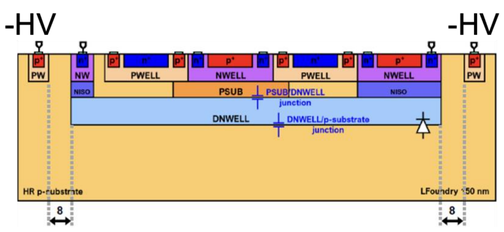
Pixel Matrix Design

Double-column architecture with FE-I3 readout
- 64 pixel columns organized in 32 double columns
- To reduce crosstalk noise:
  - Digital signal lines are in the middle
  - Analog signals are on the side
  - Shielding lines between digital lines
- Share analog and digital lines within double column to save area
- Two metal layers form a power mesh to minimize voltage drop
- Readout follows the FE-I3 style (pixel on the top has the highest read priority)
- Each pixel can be configured through a shift-register chain inside each double column

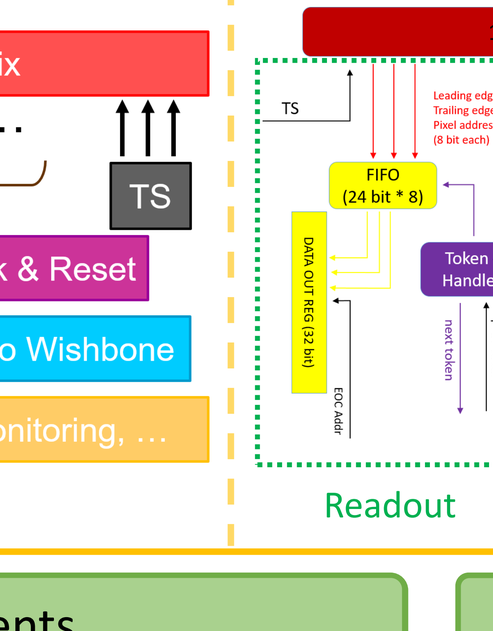


2 x 2 pixels inside double column

Large fill factor DMAPS pixel
- Analog Front-End (AFE) and Digital Electronics (DE) are embedded in separate wells to minimise crosstalk noise
- Each pixel includes:
  - Pre-amplifier
  - High-pass filter
  - Discriminator
  - 4-bit trim-DAC
  - Readout logic
  - 8-bit configuration register
  - Capability to mask noisy pixels



- Pixel provides timestamps of leading and trailing edges of discriminator output, and pixel column address

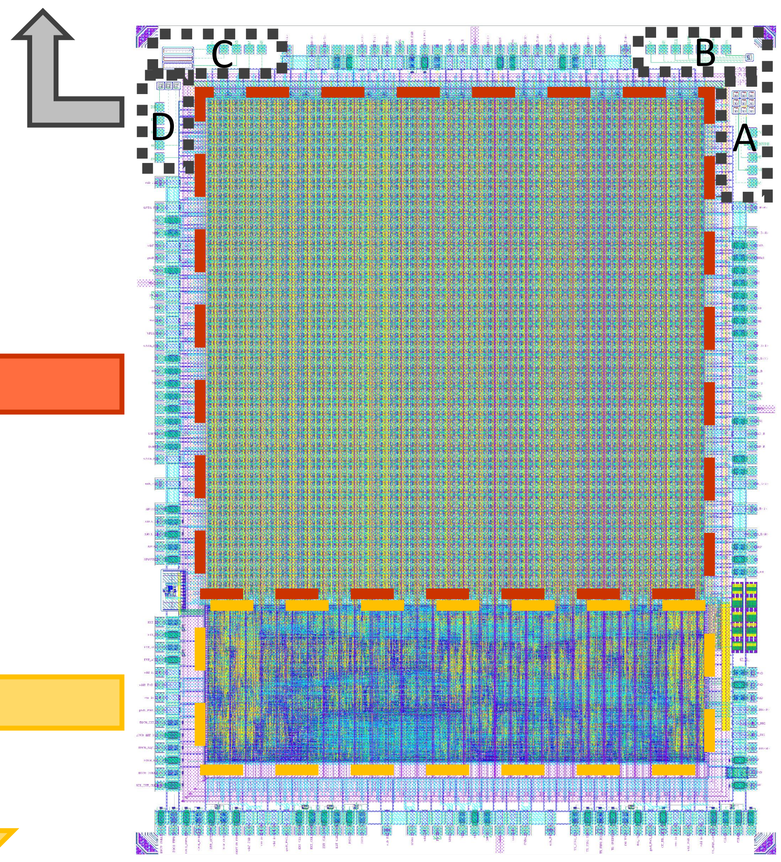


Advanced Test Structures

A) eTCT: Mini 3x3 pixel matrix for timing and charge measurements using edge-TCT

B) Capacitance: Single sensing diode for measuring capacitance of a single pixel

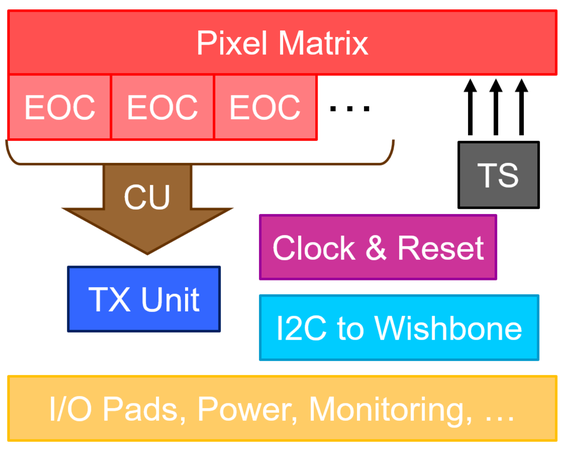
C) + D) TSC: Two different layouts for Thermally Stimulated Current (TSC) measurements for defect characterization.



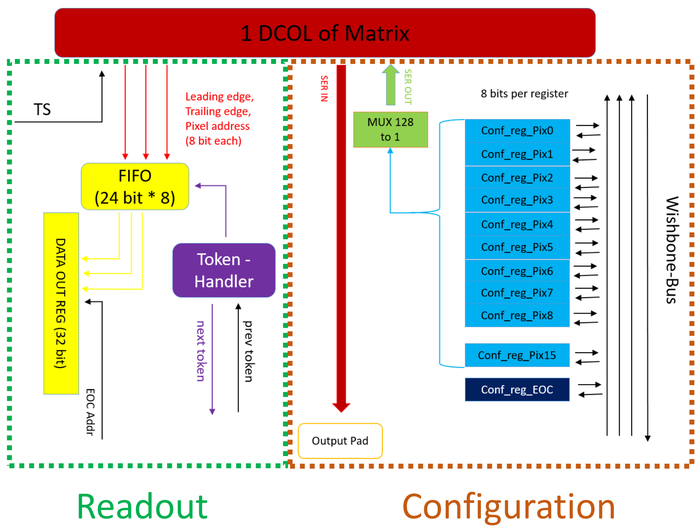
Digital Readout Design

Periphery: Peripheral electronics for readout and configuration

- 1 End of Column (EOC) per double column to readout and configure pixels
- Control Unit (CU) to push data from EOCs to readout bus: 32-bit data bus
- Transmission unit (TX Unit): De-randomization of EOC data, framing, encoding and serialization; read-out at 640 MHz
- Common timestamp generator (TS): fanned-out into all double columns
- I2C to wishbone controller: convert external I2C commands to internal wishbone commands



EOC: Configuration and readout of one double column



- 16 registers (8-bit) for pixel configuration: MUXed into serial stream
- 1 register (8-bit) for EOC configuration
- Serial read-back
- A 24-bit wide FIFO for pixel data: De-randomization of all pixel data in one double column
- Single 32-bit register for data readout: (fixed) EOC address attached to data
- Combinatorial token-handler for priority logic of EOC: Highest address readout first (rolling shutter)

Designers and Acknowledgements

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RD50-MPW3 papers

E. Vilella, Development of High Voltage-CMOS sensors within the CERN-RD50 collaboration (VERTEX2021)

P. Sieberer, et.al., Design and Characterization of Depleted Monolithic Active Pixel Sensors within the RD50 Collaboration (VCI2022)