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RD50-MPW3: A fully monolithic digital CMOS sensor for future tracking detectors

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The CERN RD50 CMOS working group develops the RD50-MPW series of monolithic CMOS sensors for potential use in future high luminosity experiments such as HL-LHC and FCC-hh.
In this contribution, we will present an overview of the RD50 High Voltage-CMOS activities, focusing on the design of RD50-MPW3, the latest chip of this series, and the readout electronics beyond the chip. We will give a detailed overview of the pixel matrix and the digital peripheral readout. We will discuss the challenges the design presented and how we solved them, together with the first laboratory evaluation results of the chip.

Summary (500 words)

Within the RD50-MPW series, we have developed three chips so far with RD50-MPW3 being the latest. This chip was submitted for fabrication in December 2021 and the delivery is expected in July 2022. The ASICs are fabricated in the LFoundry 150 nm process using a high substrate resistivity up to ˜3 kΩ·cm.

RD50-MPW3 aims to be one of the first full monolithic digital tracking sensors to be used in a high radiation environment without the need of a complicated DAQ framework. This chip keeps the well working analog part of its predecessor RD50-MPW2, completed by an in-pixel digital logic and an optimized peripheral readout for effective pixel configuration and fast serial data transmission. The chip comprises a matrix of 64x64 pixels arranged in 32 double-columns (DCOLs).

Pixel size of the analog matrix is 62 µm x 62 µm to embed the analog and digital readout electronics within the collection electrode. Post-layout simulations of a single pixel show a power consumption of 22 µW per pixel and 9 ns time walk. The matrix readout is based on the column drain architecture (FEI3-style). For each double column, an End of Column (EOC) circuit is implemented, providing a first FIFO for buffering data of the attached DCOL. Data from these 32 FIFOs is pushed into another 128 words deep FIFO for transmission. Before serialization, the data is framed and encoded (Aurora 8bit-10bit) to guarantee a stable readout. Serialization happens at 640 MHz and the data is pushed out of the chip using a single differential readout line. Configuration of the pixel is realized using an I2C interface. An I2C to wishbone module is used to convert external I2C control signals to internally used wishbone control signals, which are then forwarded to the configuration registers in the pixels.

The resulting layout and implementation will be shown in this contribution along with the initial sensor performance evaluation. Tests on the active matrix for verifying the digital readout, such as S-curves and trimming to compensate for small offset variations in the discriminator, and on passive test structures, such as current-voltage and capacitance voltage characteristics, will be shown as well.
A DAQ framework focused on the use of the chip in test beams for tracking is currently developed and will be shortly presented. The DAQ provides two different data paths, a fast data path for recording data and a slow data path for slow control and monitoring. The latter one can also be used for low rate tests. A brief overview of the readout firmware and software will be given as well, together with the concept used for synchronizing with other detectors.

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