A Monolithic Active Pixel Sensor with Node-Based, Data-Driven, Parallel Readout for the High Energy Physics Experiment Vertex Detector

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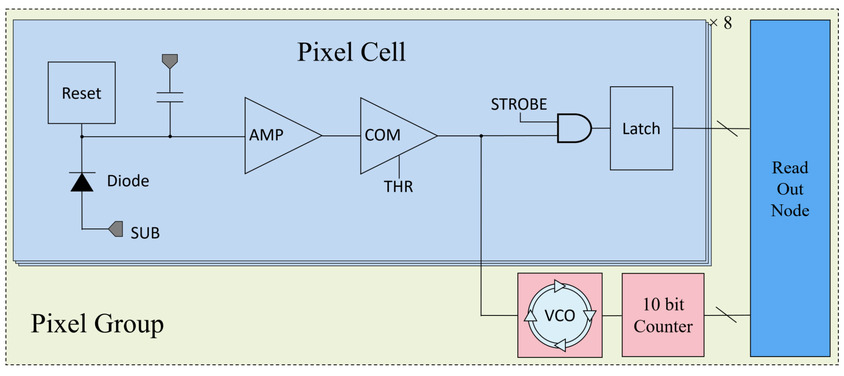
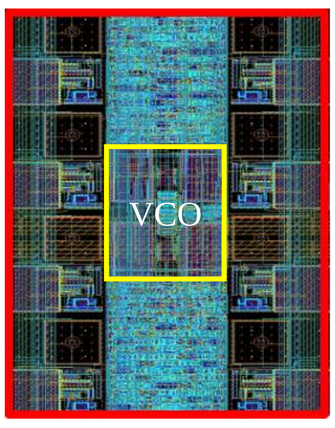
Introduction

The vertex detector in high energy physics experiment requires high spatial resolution, fast readout, and low power consumption. The Monolithic Active Pixel Sensor (MAPS) is the most promising candidate technology to satisfy all those requirements. We have developed the MAPS sensor MIC6 in a 55 nm quad-well CMOS image sensor process with a node-based data-driven readout scheme.

Super pixel group design

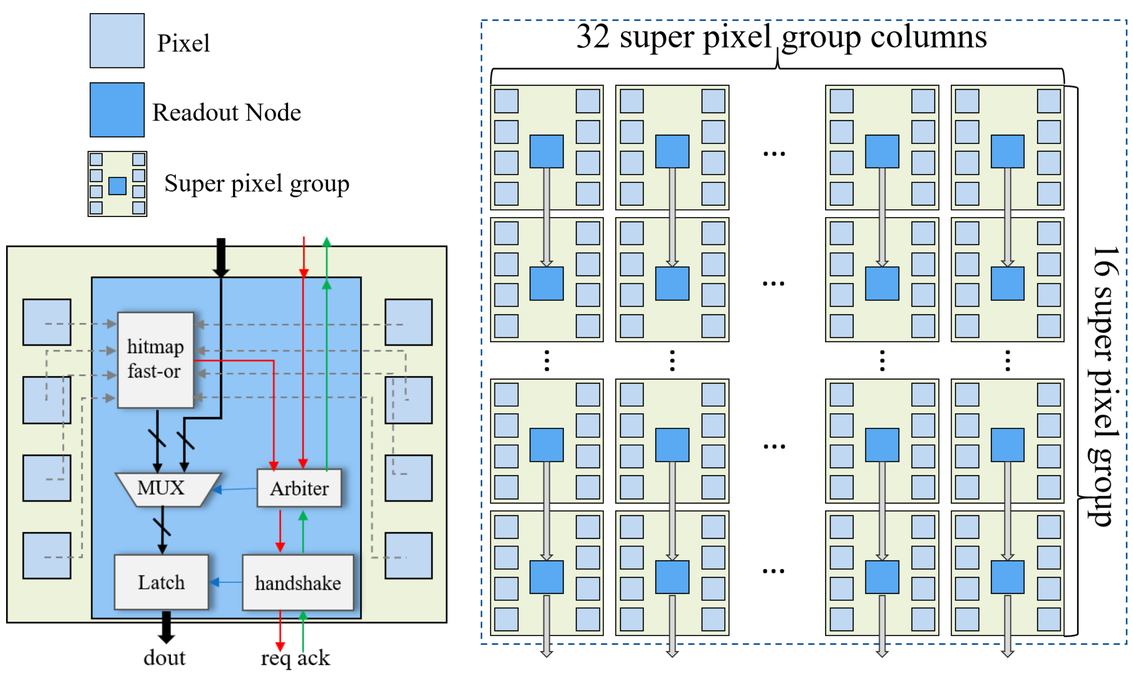
- Each super pixel group contains 8 pixels, a VCO, a 10-bit time counter, and a readout node
- Small pixel size of 23.6 μm × 20 μm
- Analog front-end and discriminator continuously active
- Digital pixel circuitry with one hit storage registers
- Front-end :
  - Same structure as ALPIDE chip (for ALICE ITS upgrade), with different parameters
  - Peaking time < 2 μs, pulse duration < 8 μs
  - ENC: ~ 5 e^-
- The VCO is used for hit arrival time measurement, and oscillates only when the super pixel group is hit
- The oscillation frequency of VCO can be configured between 100 ~ 200 MHz



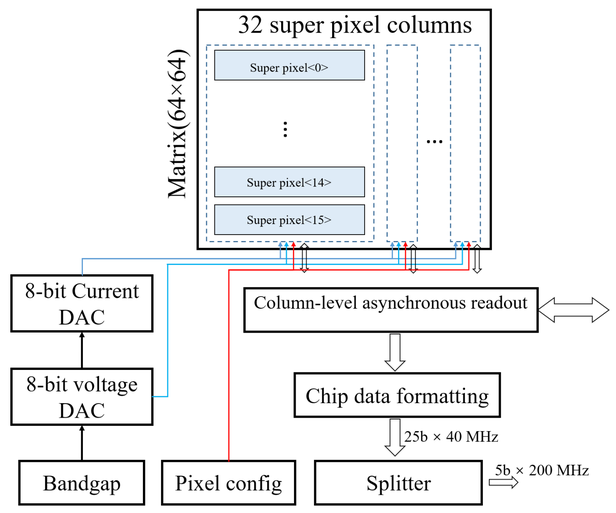


Pixel array read-out

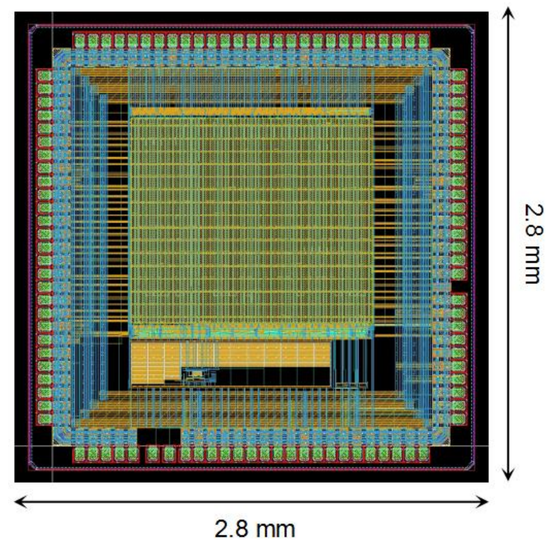
- Node-based readout:
  - 4×2 pixels form a super pixel group
  - Each super pixel group shares a node of sparse readout logic circuit
  - The hit information is asynchronously transmitted to the bottom of the double-column through the readout nodes
  - Asynchronous data driven based on four-phase handshake
- When a super pixel group is hit, 22 bit data will be generated, including 4-bit super pixel group address, 10-bit time counter and 8-bit hit shape



Prototype overview



Block diagram of the prototype

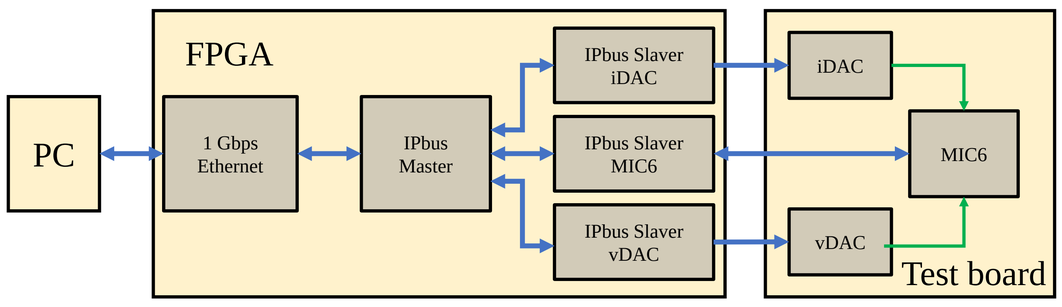


Prototype layout

- Die size: 2.8 mm × 2.8 mm
- 64 × 64 pixels with size of of 23.6 μm × 20 μm
- Readout speed: 40 MHz/super pixel group in the worth case
- Chip power: 40 mW/cm^2
- No memory in the periphery, data readout through parallel interface

The test system

- The test system is being developed and consists of a test board, a Kinex-7 FPGA and control software. The test firmware and software are based on IPbus.
- The test commands from the control software on PC are received by the 1 Gbps TCP/IP module and then transmitted to IPbus master. The commands from the IPbus master are sent to one of the IPbus slavers. The current DAC, voltage DAC and the MIC6 are configured by the respective IPbus slaver.
- The data flow of the test system is opposite to the flow of test command. The output data of MIC6 are transmitted to PC through ipbus slave, ipbus master and Ethernet interfaces in turn.



Conclusions

We have designed a CMOS pixel sensor prototype based on a 55 nm Quad-well CMOS Image Sensor process for the high energy physics experiment vertex detector application. A new node-based, data-driven, parallel readout architecture is implemented to achieve high spatial resolution, fast readout, and low power consumption.

The prototype has been fabricated and returned from the foundry recently. The test system has been developing. The prototype is expected to be characterized in the December 2022.

Acknowledgments

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