A high speed phase locked loop of a pixel readout ASIC for the CSR external-target experiment

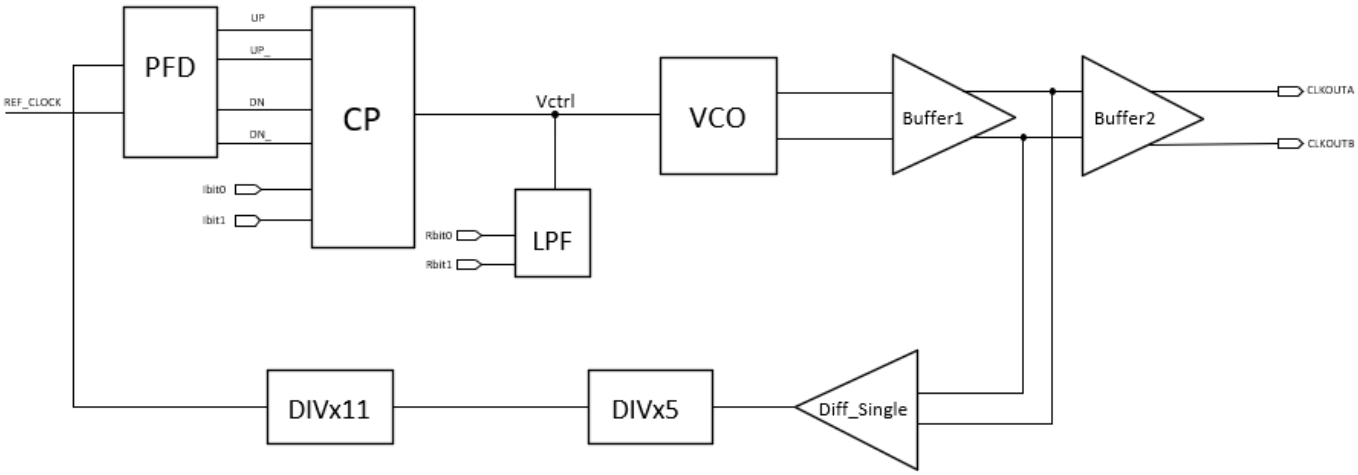

figure. 1. Block diagram of phase locked loop

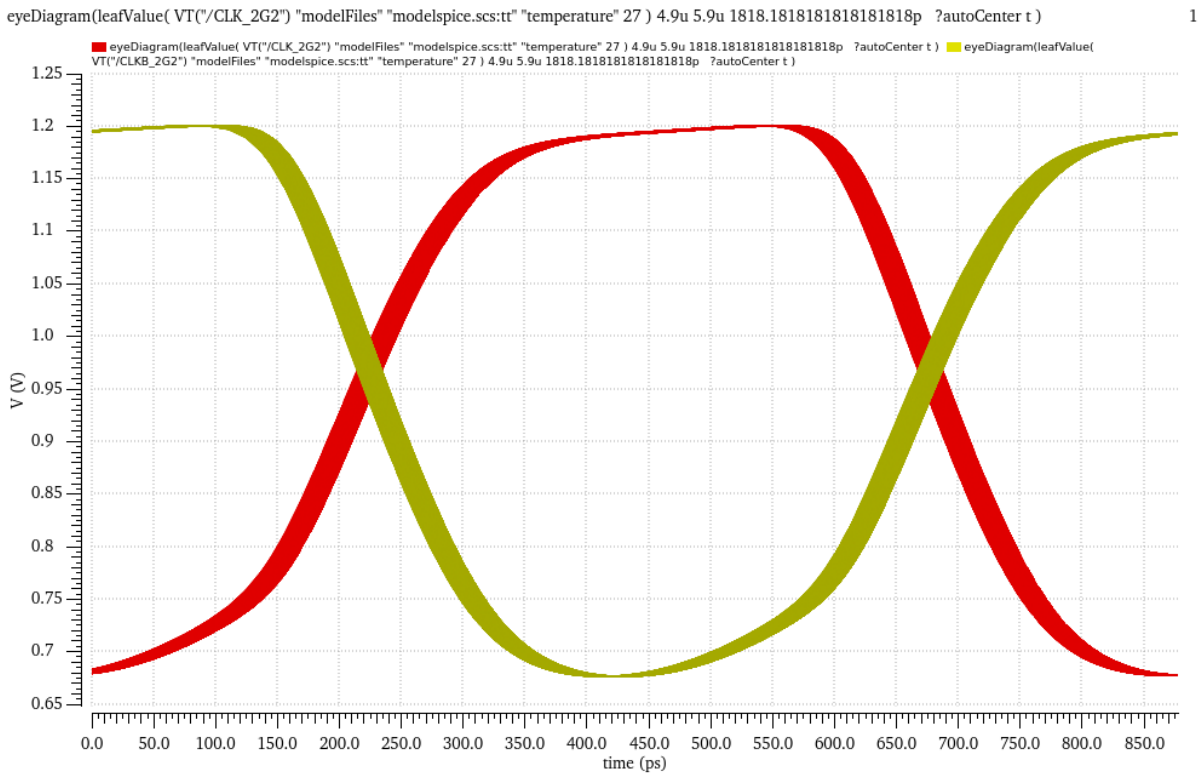

figure. 2. Post-simulation: Input 20MHz clock output 1.1GHz clock jitter is 20ps

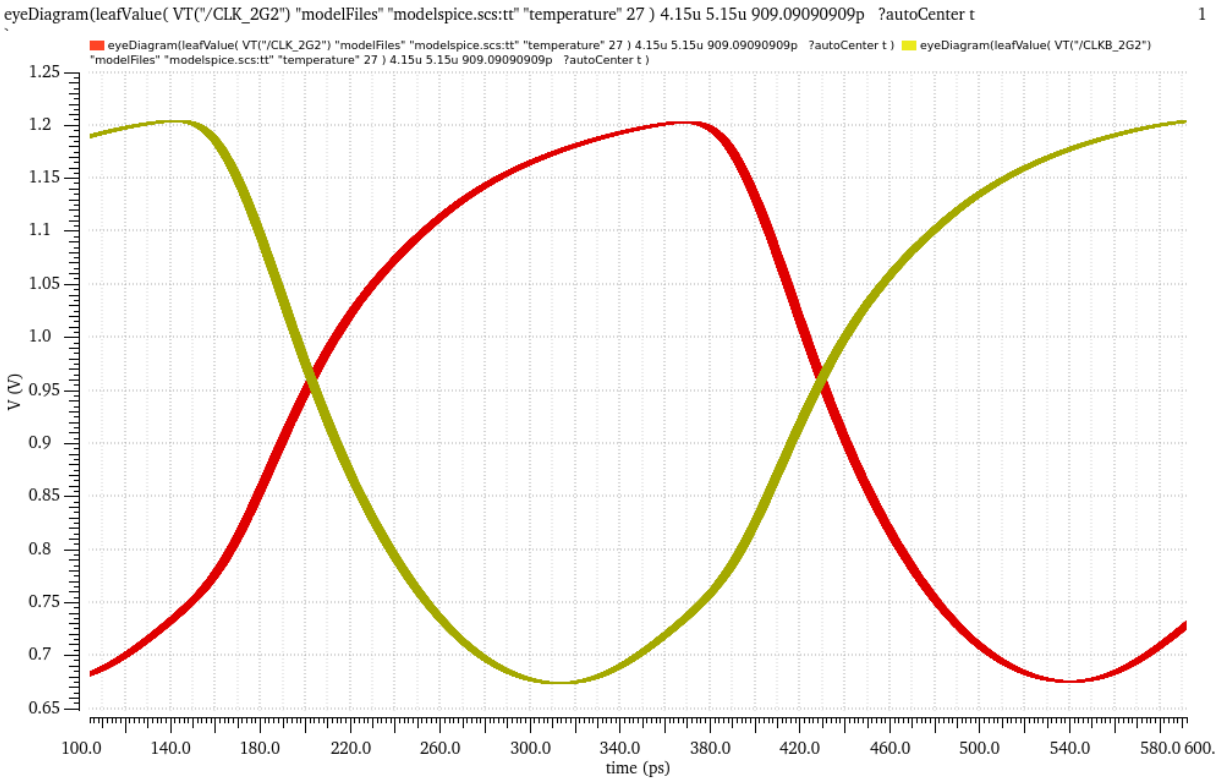

figure. 3. Post-simulation: Input 40MHz clock output 2.2GHz clock jitter is 3.7ps

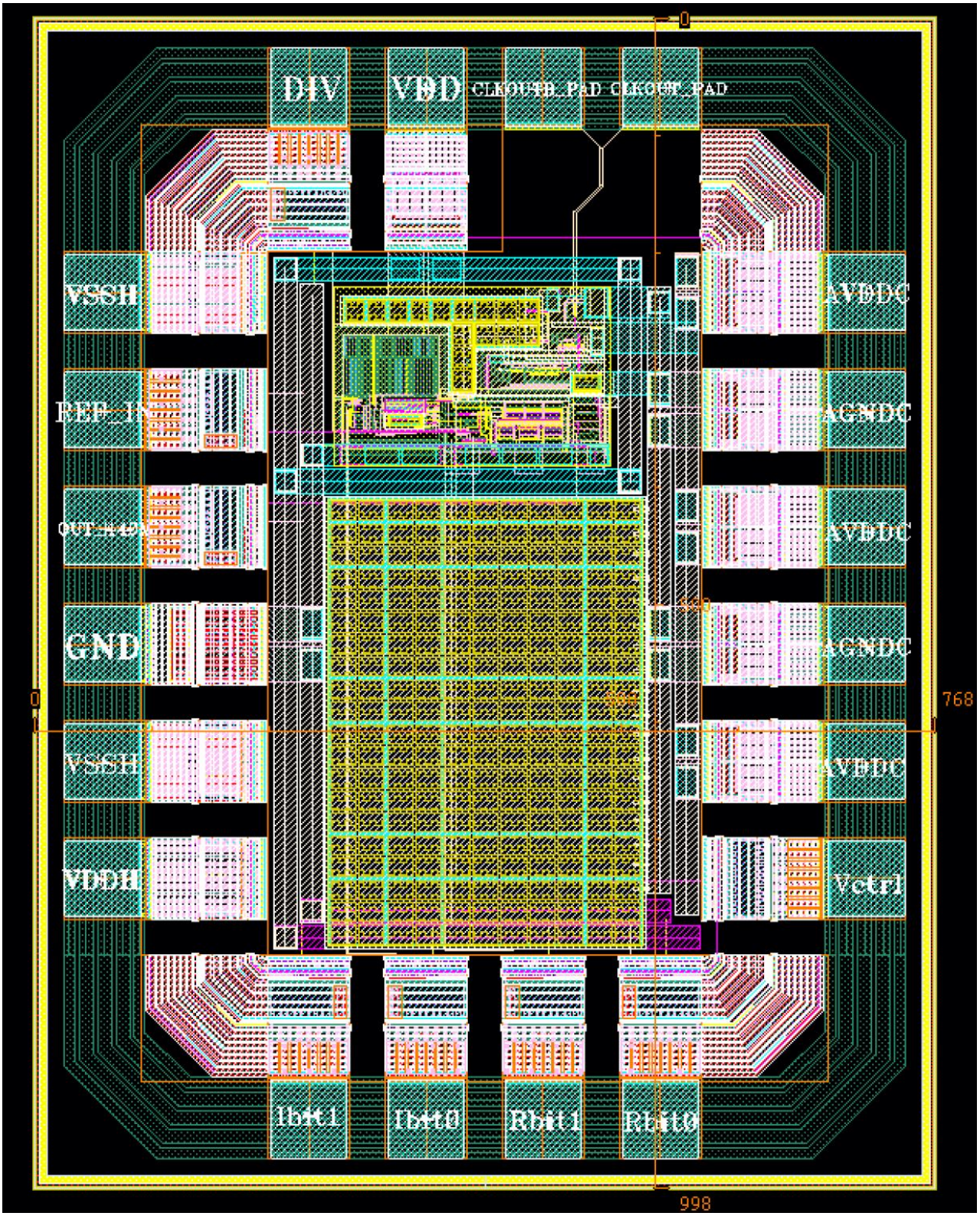

figure. 4. Layout of the pll, Area 1×0.8mm

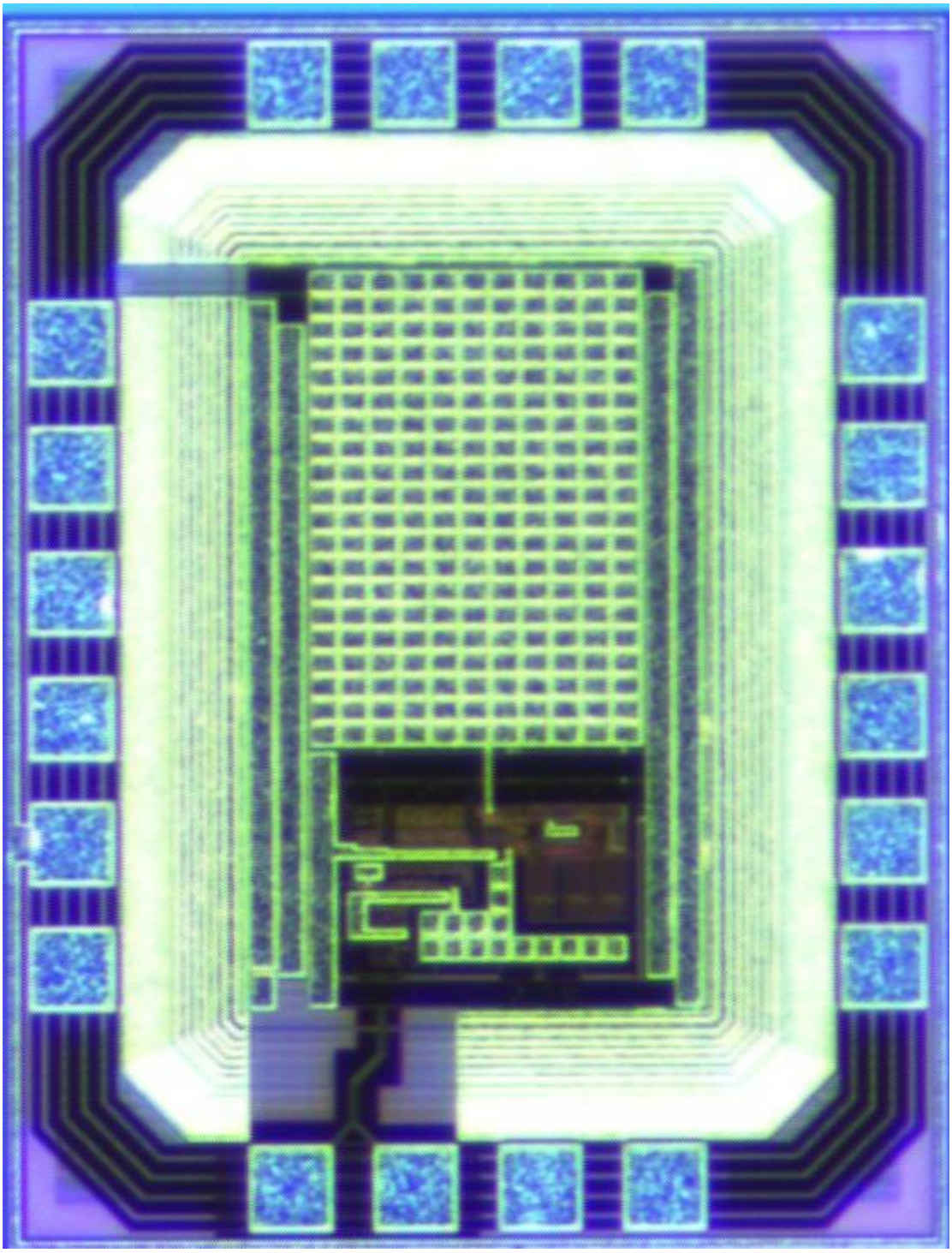

figure. 5. Tape-out successful PLL chip