A high speed phase locked loop of a pixel readout ASIC for the CSR external-target experiment

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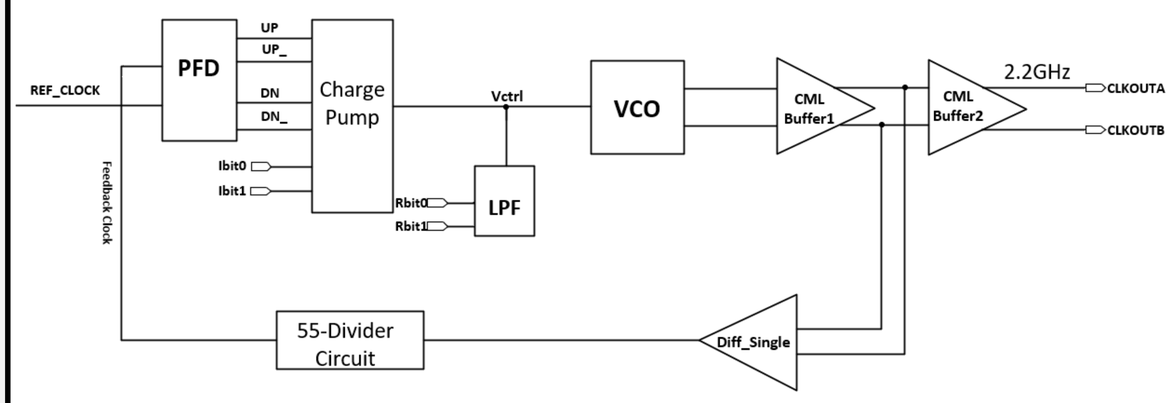
Abstract

We present a high speed Phase Locked Loop (PLL) which is designed to provide high speed clock for a pixel chip to transmit the serial data off chip. The pixel chip is designed to read out the charge of a beam monitor which is part of the CSR external-target experiment at HIRFL in China. The PLL consists of a differential ring oscillator, a digital divider, three-state phase frequency detector, a current charge pump and a second-order loop filter. Measurements show that the peak-to-peak differential amplitude is 244 mV with the duty cycle of 50.3%. At 2.2GHz, the total jitter is 36.72ps with the RMS jitter of 1.16ps and the phase noise is -90.77dBc/Hz @ 1MHz offset.

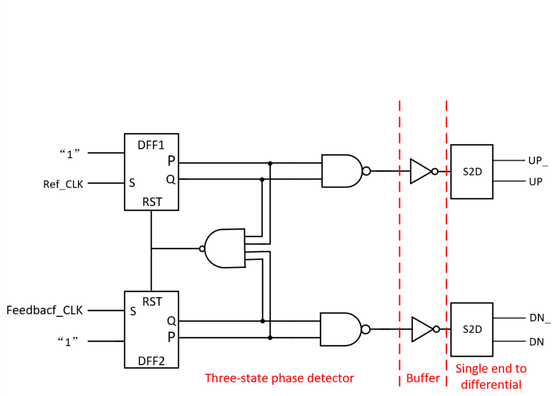
Introduction



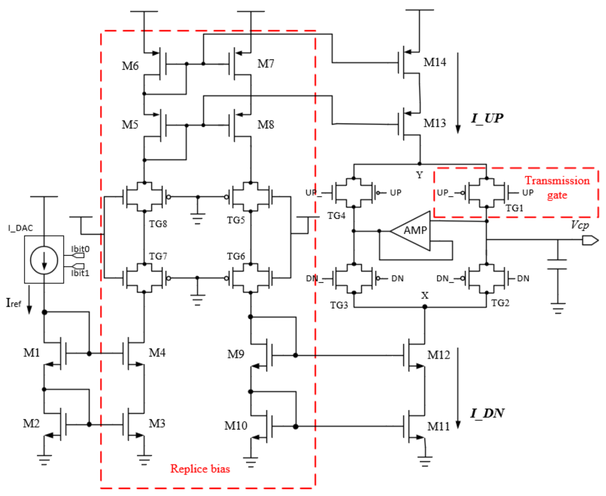
Block diagram of PLL

- The PLL consists of a differential ring oscillator, a differential to single-ended circuit, a digital divider, three-state phase frequency detector, a current charge pump, a second-order loop filter and a CML output buffer.
- The PFD detects the phase difference between the reference clock signal and feedback clock signal, and then transforms it into an electrical signal. The CP controlled by the up or down signal generated by the PFD, will source current to the LPF or sink current from the LPF, resulting in the VCO control voltage. The control voltage is used to fine-tune change the oscillating frequency of the VCO finally, The VCO sends its output through a differential to single-ended circuit to a 55 divider circuit to maintain closed-loop stability.

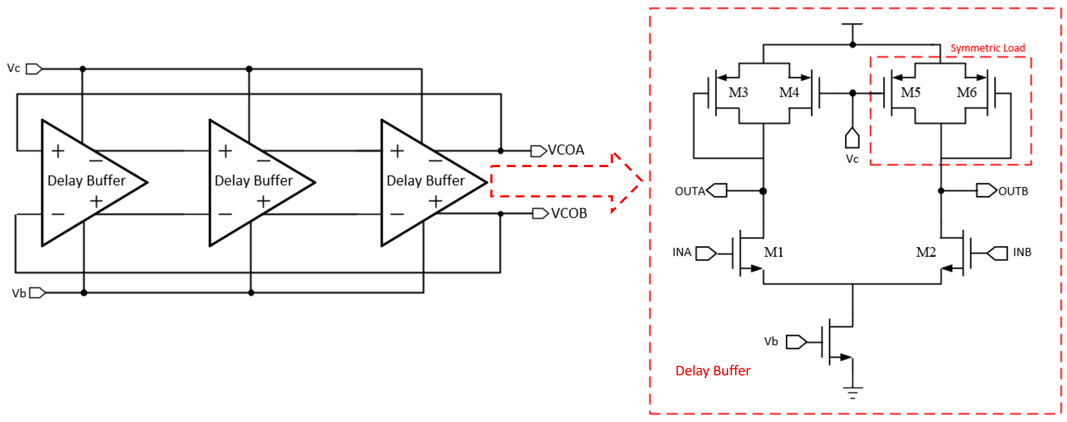
Main modules of PLL



PFD circuit



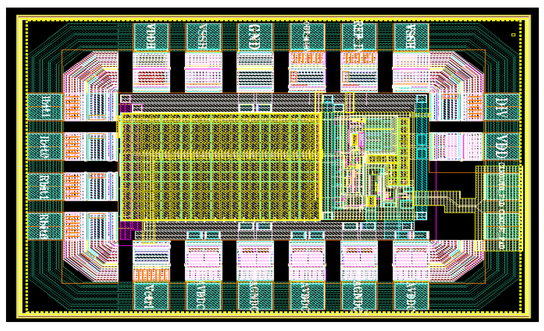
Charge pump circuit



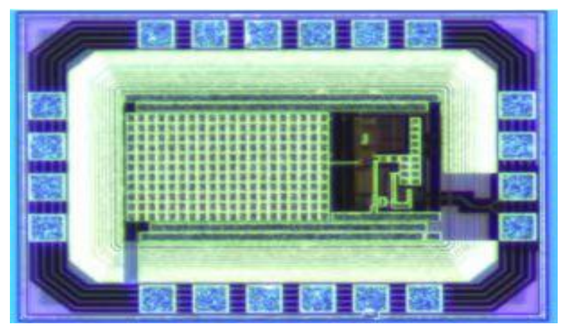
VCO circuit

- Drain-switched current type charge pump. In order to decrease the effect from the process, voltage and temperature, an adjustable reference current generated by a 2-bit current digital-to-analog converter is used.
- A voltage- controlled oscillator which is composed of three-stage differential delay unit is adopted. A symmetric load is adopted in the differential delay unit to reduce the differential impedance variation caused by the common noise of the system.

PLL photograph & layout

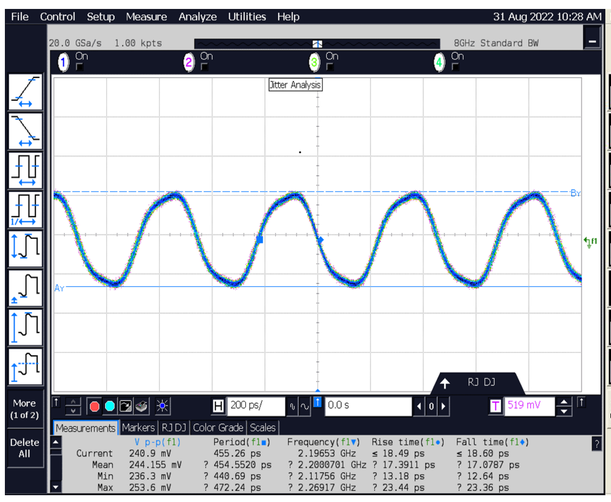


layout

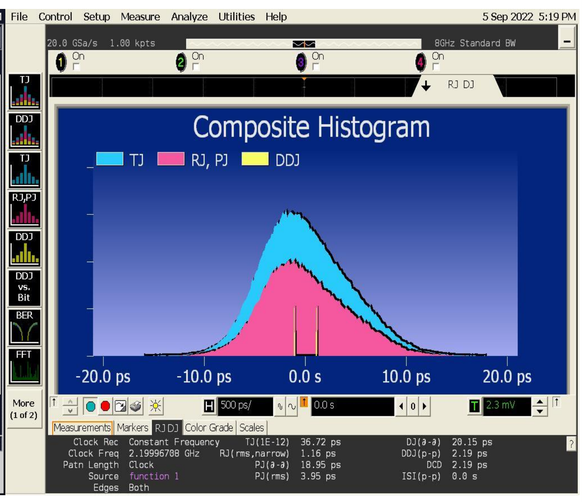


microphotograph

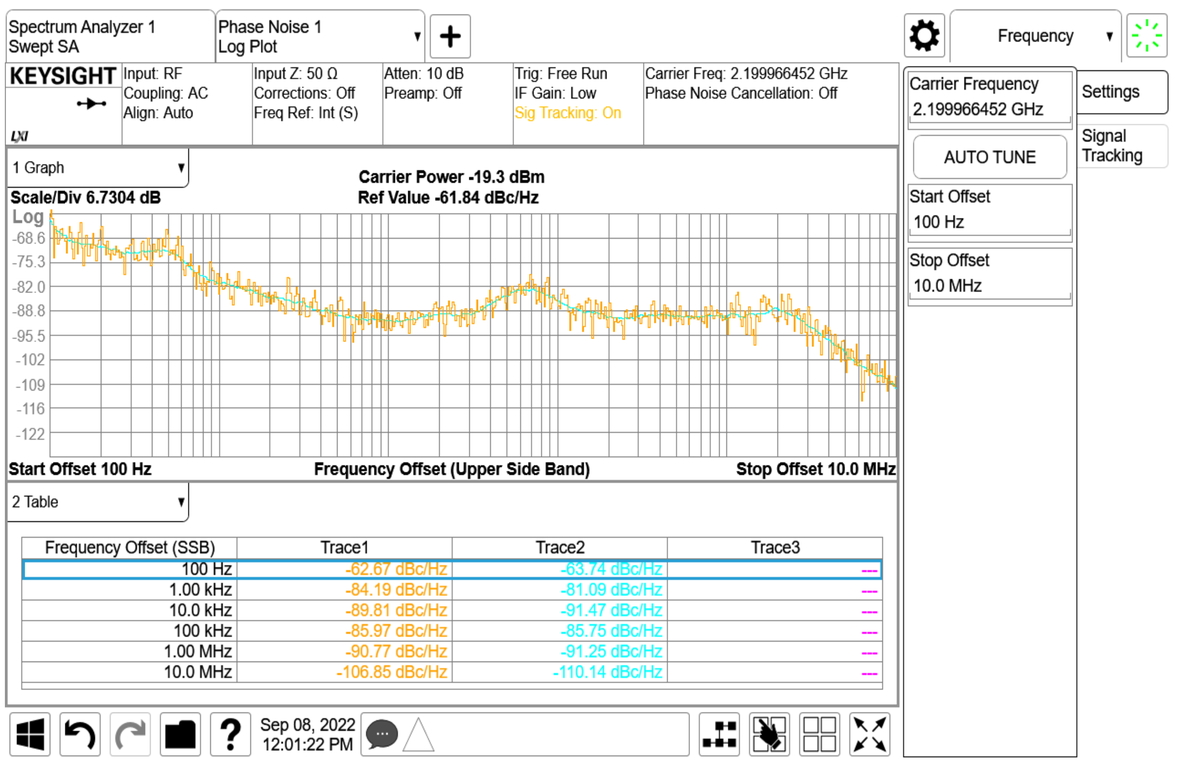
Measurement Results



Waveform of the PLL output clock



Jitter analysis results



Phase noise performance result

- **Measurement result**: The test results shows that the peak-to-peak differential amplitude is 244 mV with the duty cycle of 50.3%. At 2.2GHz, the total jitter is 36.72ps with the RMS jitter of 1.16ps and the phase noise is -90.77dBc/Hz @ 1MHz offset.

Summary and Outlook

A high speed phase locked loop of a pixel readout ASIC for the CSR external-target experiment， which has been manufactured in a standard CMOS 130 nm process, was successfully implemented and proven to function correctly. It has a clock jitter of 36.72ps at 2.2GHz and the phase noise is -90.77dBc/Hz @ 1MHz offset.. We will also research and design a new high-speed phase-locked loop with even lower jitter in the future.