Contribution ID: **157** Type: **Poster**

A high speed phase locked loop of a pixel readout ASIC for the CSR external-target experiment

Tuesday 20 September 2022 16:40 (20 minutes)

We present a high speed Phase Locked Loop (PLL) which is designed to provide high speed clock for a pixel chip to transmit the serial data off chip. The pixel chip is designed to read out the charge of a beam monitor which is part of the CSR external-target experiment at HIRFL in China. The PLL consists of a differential ring oscillator, a digital divider, three-state phase frequency detector, a current charge pump and a second-order loop filter. The simulations show that the output clock frequency is 1.1 GHz or 2.2GHz with a jitter of ˜4ps

Summary (500 words)

The Cooling Storage Ring (CSR) External-target Experiment (CEE) is being developed at the Heavy Ion Research Facility in Lanzhou (HIRFL) in China. It is a large-scale nuclear physics experiment and operates in the GeV energy region. This experiment is designed to study the nuclear matter phase structure at the low temperature and low baryon density, hence facilitating frontier scientific research in the field of high energy physics. The beam monitor is part of the CEE detector, measuring the position and the time information of the incident particles. A pixel ASIC is also being developed for the beam monitor to read out the charge. A high speed Phase Locked Loop (PLL) presented in this paper is designed to provide high speed clock for the pixel ASIC to transmit the serial data off chip.

The PLL consists of a differential ring oscillator, a digital divider, three-state phase frequency detector, a current charge pump and a second-order loop filter. A voltage- controlled oscillator which is composed of three-stage differential delay unit is adopted. A symmetric load is adopted in the differential delay unit to reduce the differential impedance variation caused by the common noise of the system. And also, the impedance can be adjustable through changing the gate voltage. Therefore it can improve the clock performance. The voltage-controlled differential oscillator generates a clock with a frequency of 1.1GHz or 2.2GHz. The frequency of the reference clock is 20MHz or 40MHz. Therefore, the clock generated from the oscillator is divided by 55 and then the clock after division is fed into the phase frequency detector, which is composed of an edge detector and a single end to difference. A transmission gate is added to decrease the phase difference between the differential signal. In order to eliminate the dead zone of the phase detection, some delay units is added in the edge detector. A folded cascode current source based on switching bridge mode is adopted for the charge bump. In order to decrease the effect from the process, voltage and temperature, an adjustable reference current generated by a 2-bit current digital-to-analog converter is used. The output voltage of the charge bump is fed into a two-order loop filter which is a RC passive low pass filter. The stable output voltage is fed into the oscillator to adjust the oscillation frequency.

The PLL has been implemented in the pixel ASIC. And also, a test chip of the PLL is designed to test its performance. The area of the test chip with some additional test PADs is about 280μmx530μm. The simulations show that the output clock frequency is 1.1 GHz or 2.2GHz with a jitter of ˜4ps. The test chip has been manufactured and come back to the lab. A test printed circuit board is being designed. The test work will be done in detailed. In the conference, we will present the detailed test results.

Primary authors: HU, Zhengyu; GAO, Chaosong (Central China Normal University); ZHU, Pengzhen; LIU, Jun (Central China Normal University CCNU (CN)); QIAO, Yuxin; SUN, Xiangming (Central China Normal University); HUANG, Guangming

Presenters: HU, Zhengyu; GAO, Chaosong (Central China Normal University)

Session Classification: Tuesday posters session

Track Classification: ASIC