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A four-channel front-end readout ASIC for high hit rate gas detector

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The High-density High-precision High-speed Front-End Electronic (HFEE) is widely used in the high hit rate gas detectors. The design and characterization of a HFEE prototype is presented in this paper. The prototype chip is composed of four channels and each channel consists of a charge-sensitive preamplifier, a pole-zero cancellation circuit, a S-K filter and a gain amplifier. The simulations show that the equivalent noise charge is about 779e- + 3.592/pF, the non-linearity is less than 1% and the hit rate is up to 10MHz. The test work is being prepared and the test results will be presented in the conference.

Summary (500 words)

The gas detector has been widely applied in high energy physics experiments since the gas detector has the advantages of large area, high spatial and time resolution. The future application of gas detectors requires the ASICs with an amount of channels and high event rate processing capacity. In this paper, we will present a High-density High-precision High-speed Front-End Electronic (HFEE) prototype with four channels, which has been manufactured in a standard CMOS 130 nm process.

Each channel is composed of a charge-sensitive preamplifier, a pole-zero cancellation circuit, a S-K filter and a gain amplifier. The charge-sensitive preamplifier adopts a single-end folded cascode amplifier with a feedback capacitor of 500fF. The decay time can be adjusted by a bias voltage provided from off chip. The output of the charge-sensitive preamplifier is fed into a pole-zero cancellation circuit, which is composed of passive devices (one capacitor and two resistor). The pole-zero cancellation circuit is used to decrease the decay time hence reducing the pipe up effect. A S-K low pass filter follows on the pole-zero cancellation circuit to realize pule shaping. It consists of two series resistors, two capacitors and a two-stage amplifier. The last stage is a gain amplifier with a factor of two. The analog signal of each channel is driven off chip by a unity-gain buffer. The size of each channel is about 150μm x 210μm.

The size of the prototype is about 1.2mm x 2.7mm with monitoring PADs. The post simulations have been done with the whole chip extracted parasitic parameters by the calibre pex tool. The charge is injected through a capacitor of 500fF connected to the input PAD. The simulations show that the equivalent noise charge is about 779e- + 3.592/pF, the non-linearity is less than 1% and the hit rate is up to 10MHz.

The prototype chip has been manufactured and come back to our lab. The test printed circuit board has also been designed and is manufacturing in the foundry. The chip will be tested in detailed in the future one month. The test results will be presented in the conference.

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