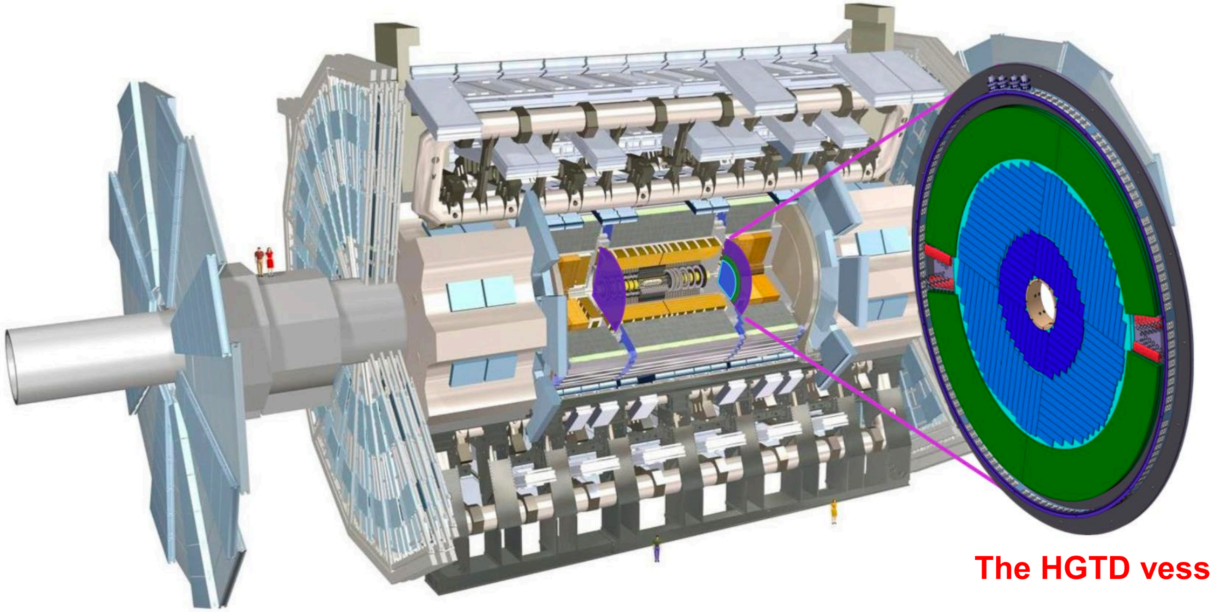
TWEPP Abstract

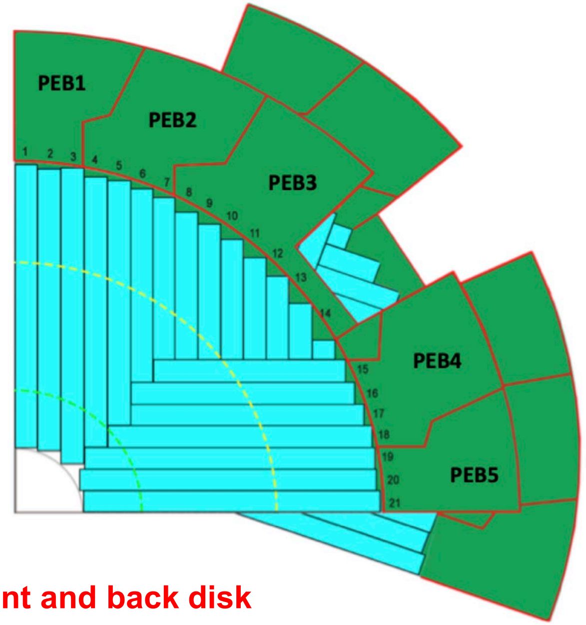
-- An Optional File for MUX64

High Granularity Timing Detector



The HGTD vessel

The ATLAS Detector



One quardrant of HGTD front and back disk

High Granularity Timing Detector (HGTD)

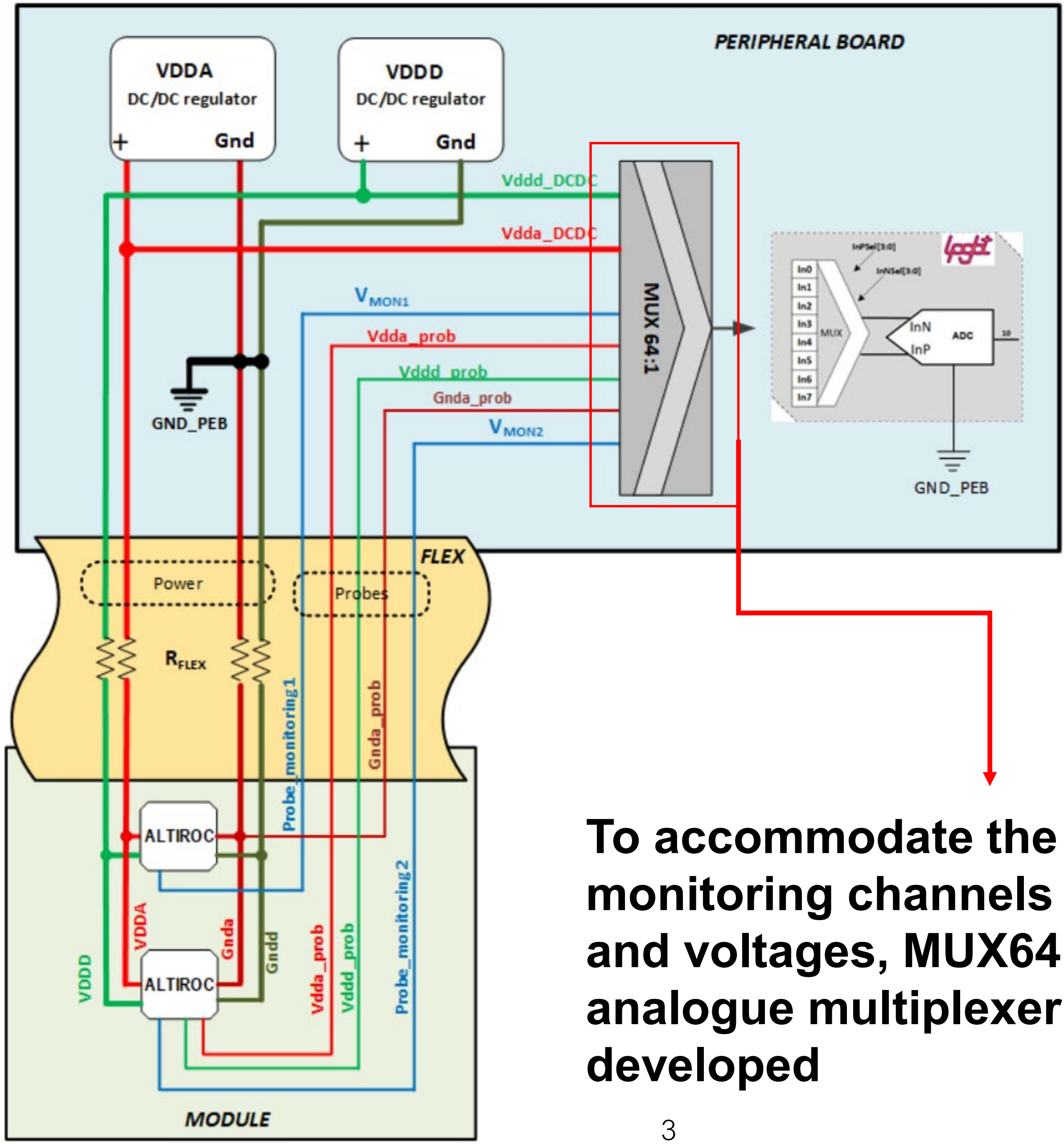
The increase of pileup will be one of the main challenges in the High-Luminosity LHC. Therefore, a High-Granularity Timing Detector (HGTD) has been proposed for the ATLAS Phase-II upgrade to mitigate the pileup effects caused by the increasing luminosity of proton-proton collision.

Two HGTD vessels will be located in the gap region between the barrel and the end-cap calorimeter, at a distance in z of approximately +-3.5m from the interaction point.

The envelope of the detector vessel has a radial extent of 110 to 1000mm. The thickness in z is 75mm, where two double-sided layers are mounted in two cooling disks with sensors and Peripheral Electronics Boards (PEB) on the front and back of each cooling disk.

The Peripheral Electronics Boards (PEB) are located at the peripheral area of HGTD, and serve as a data transmission bridge between the front-end detector modules and DAQ system, the luminosity system as well as the detector control system.

HGTD Read-out Electronics



To accommodate the large number of monitoring channels for temperatures and voltages, MUX64, a 64-to-1 analogue multiplexer ASIC has been developed

MUX64 schematic view and logic function sheet

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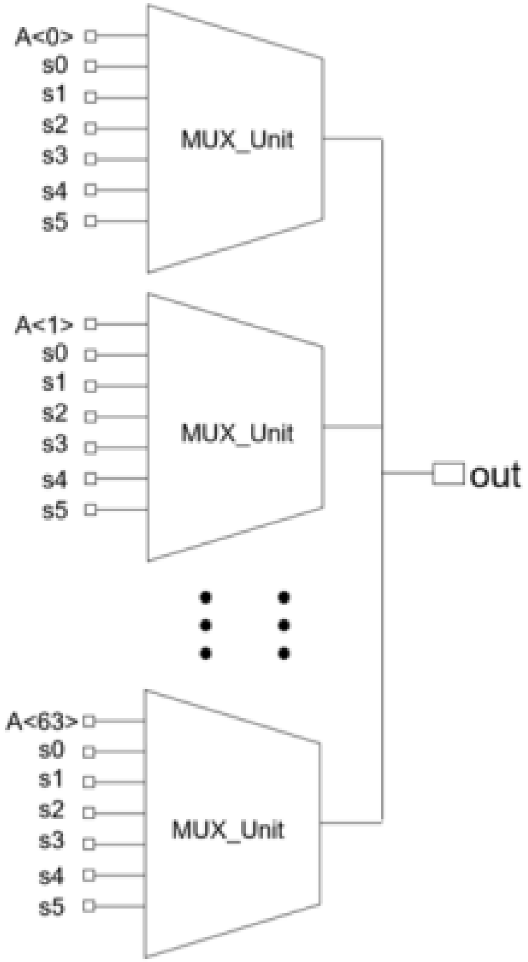
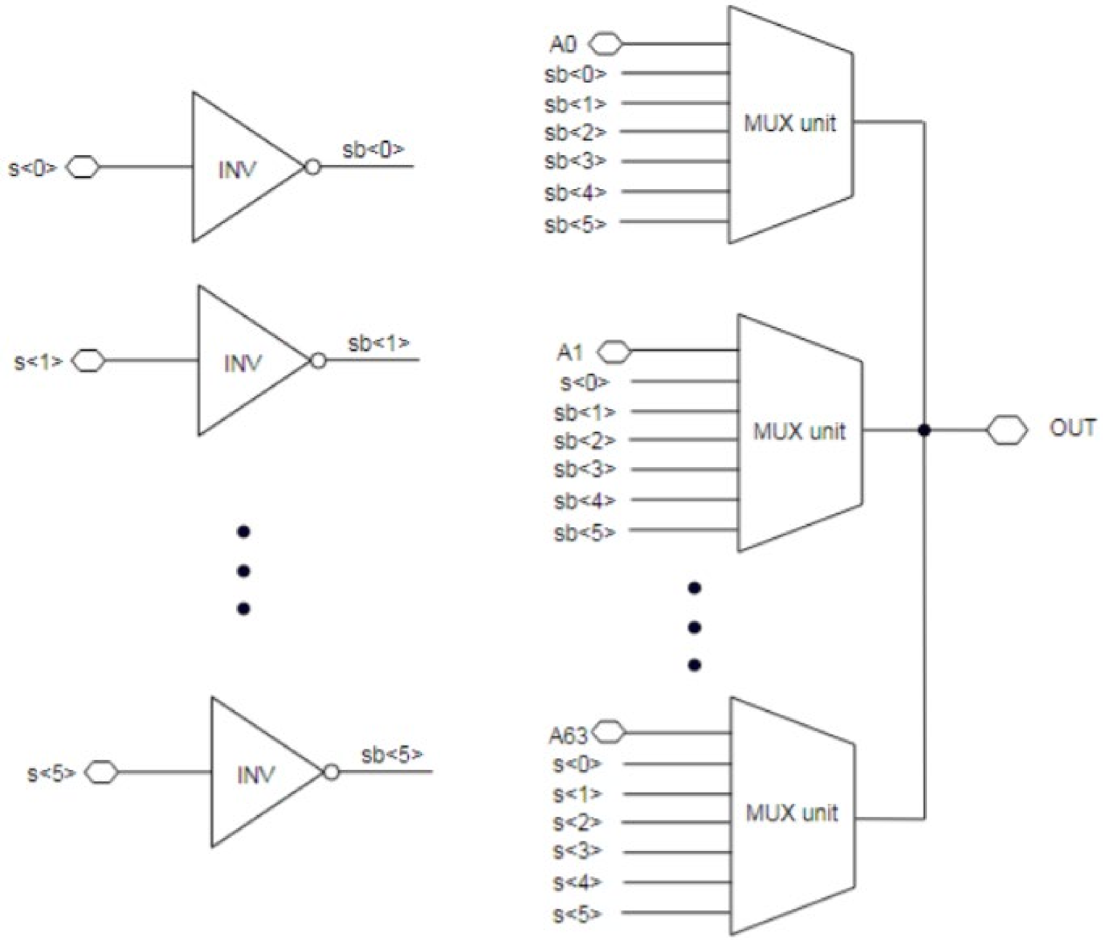


6-bit addressing

64 inputs

input	s5	s4	s3	s2	s1	s0	out
A0	0	0	0	0	0	0	A0
A1	0	0	0	0	0	1	A1
A2	0	0	0	0	1	0	A2
A3	0	0	0	0	1	1	A3
		MUX64t1 Logic Function sheet					
A63	1	1	1	1	1	1	A63

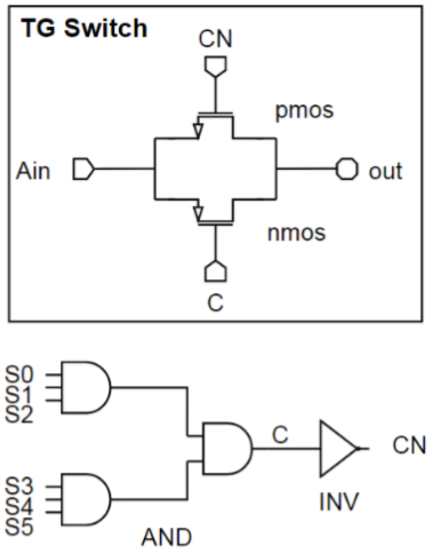
MUX64 Block diagram



6 bit control

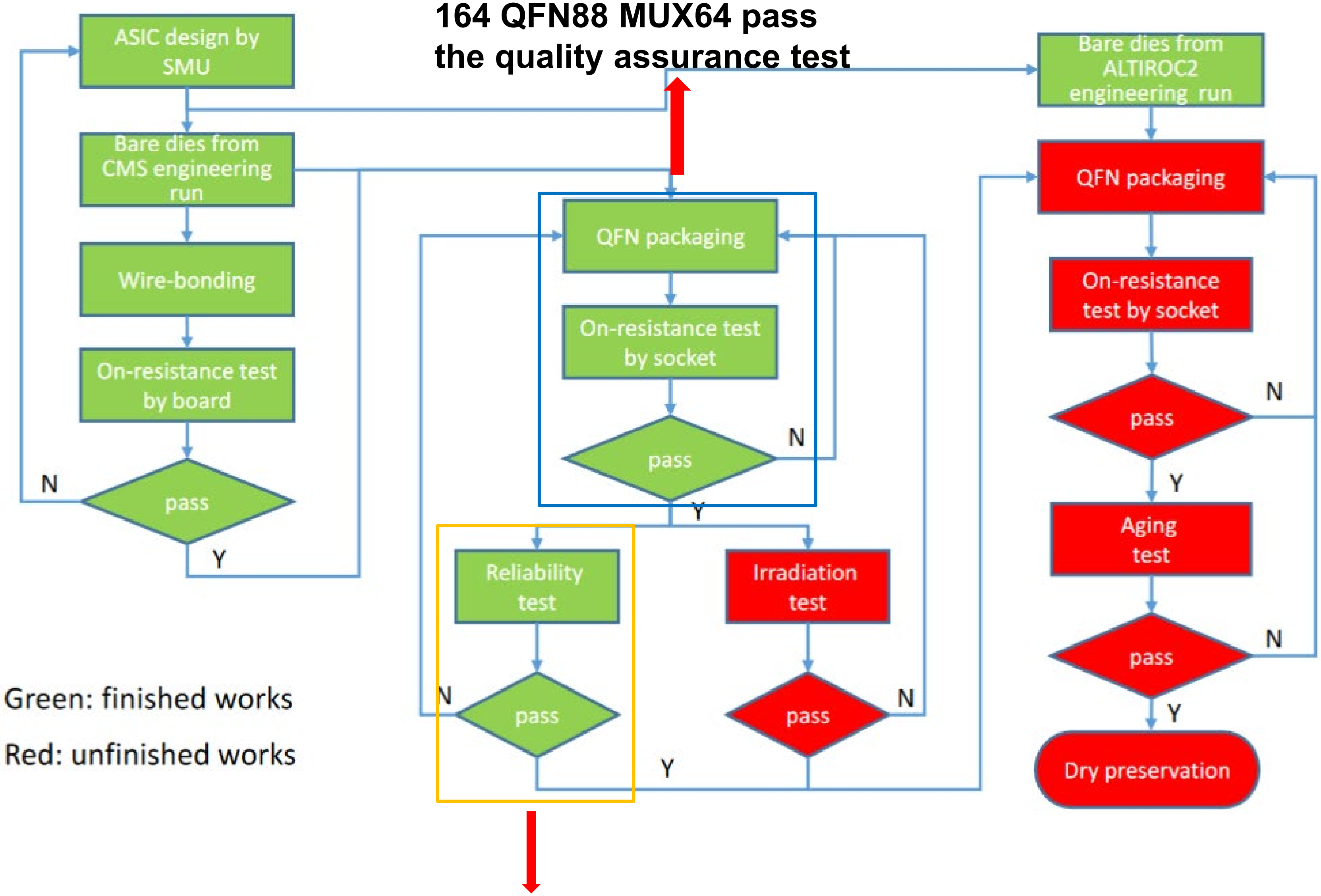
64 channel

MUX64 block diagram



Schematic of one unit, a simple transmission gate controlled by C and CN

MUX64 Technical Progress

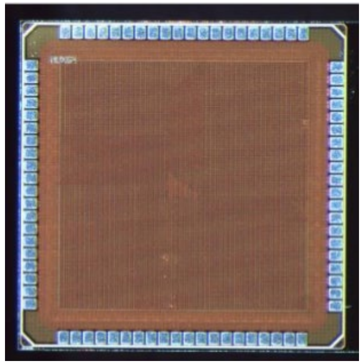


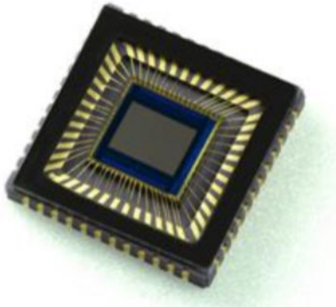
164 QFN88 MUX64 pass the quality assurance test

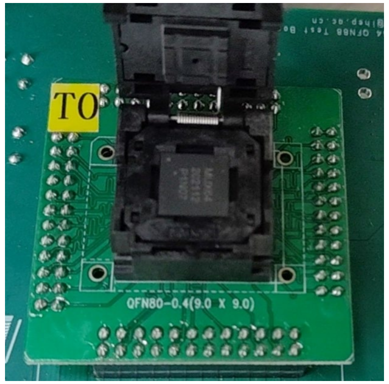
- 🟩 Green: finished works
- 🟥 Red: unfinished works

Pass first 16 days high temperature ageing test in 85℃

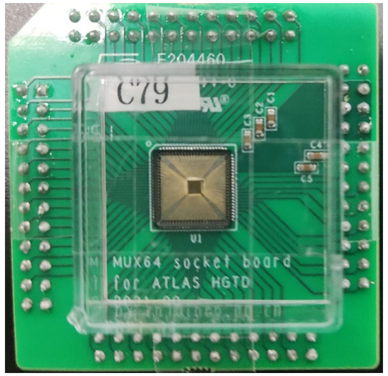
MUX64 Technical Progress


MUX64 bare dies

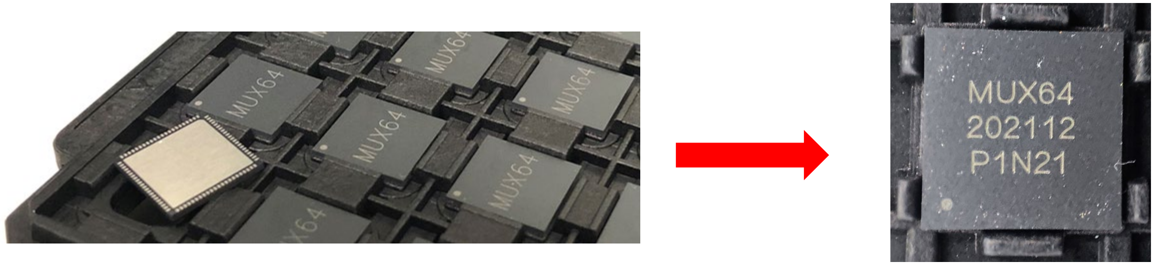

Example of the open cavity



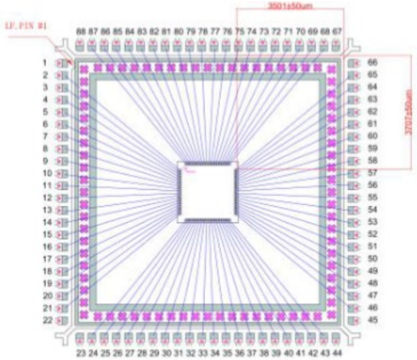
QFN88 socket adapter board

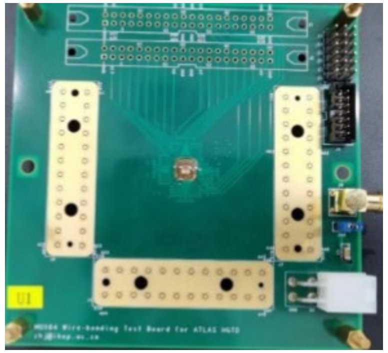


Open cavity test board



MUX64 in QFN88 package


Wire-bonding in QFN88

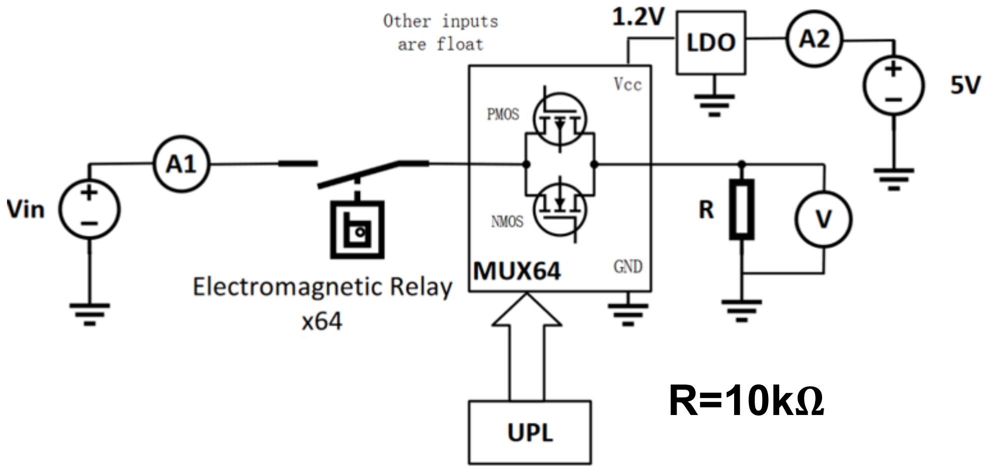


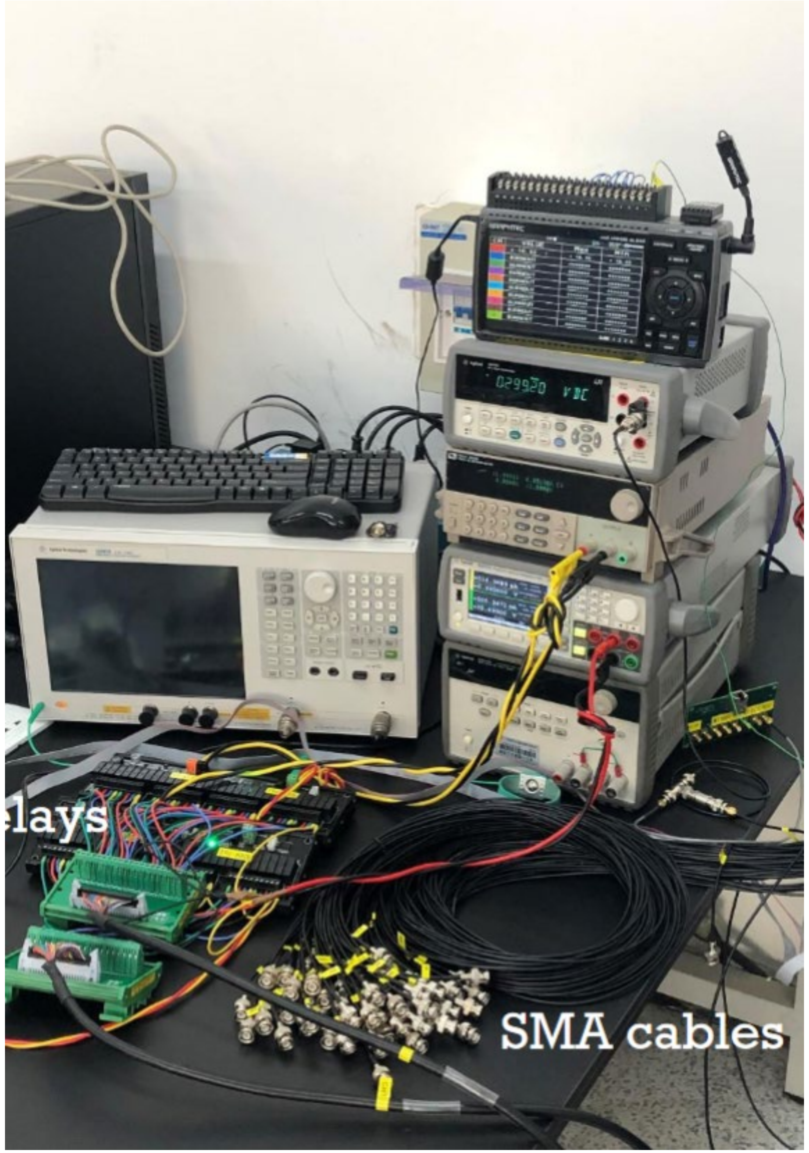
Wire-bonding test board

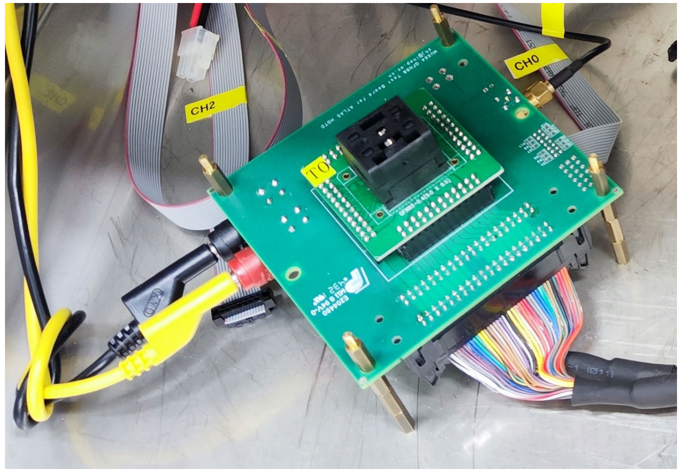
MUX64 Quality Assurance Test Setup

Automatic test system

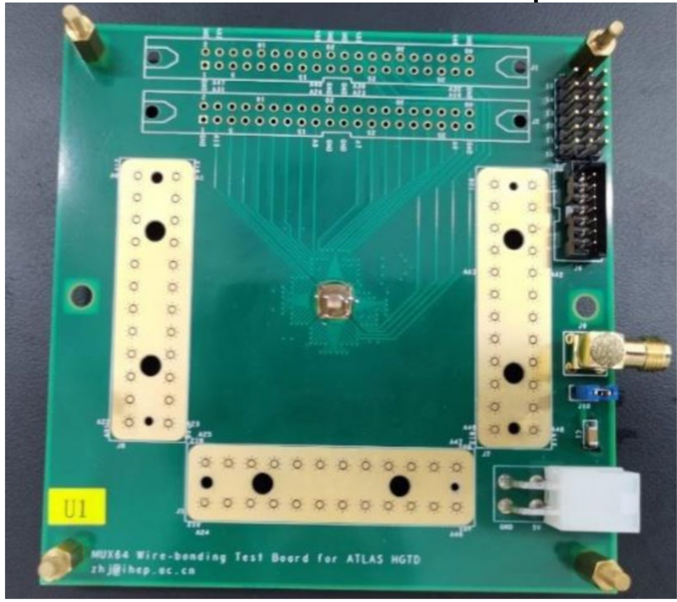
- Keysight B2912A Source Meter
  - Control & measure by Ethernet
- Angilent 34410A Digital Multimeter
  - Measure by Ethernet
- R: 10KΩ
- Use UPL to select channel of MUX64
  - Control by USB
- Use Electromagnetic relays to provide inputs
  - Control by USB
  - On-resistance < 0.1Ω







MUX64 testing board
+ QFN88 socket adapter



MUX64 wire-bonding testing board

Quality Assurance Test for QFN MUX64

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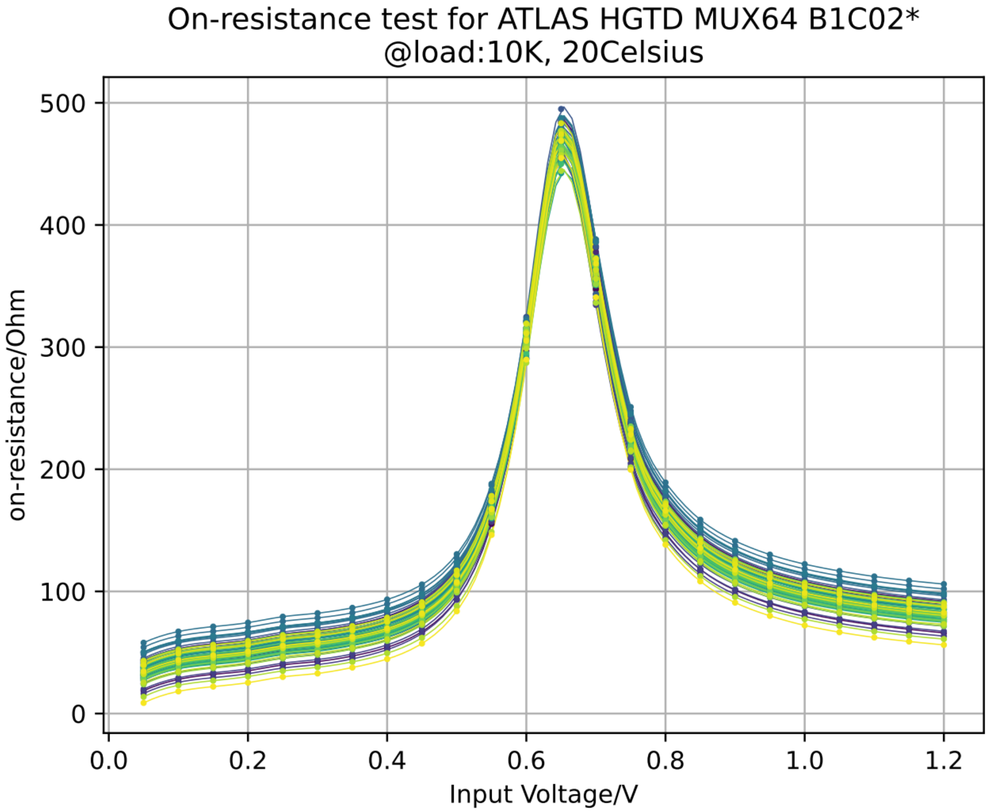
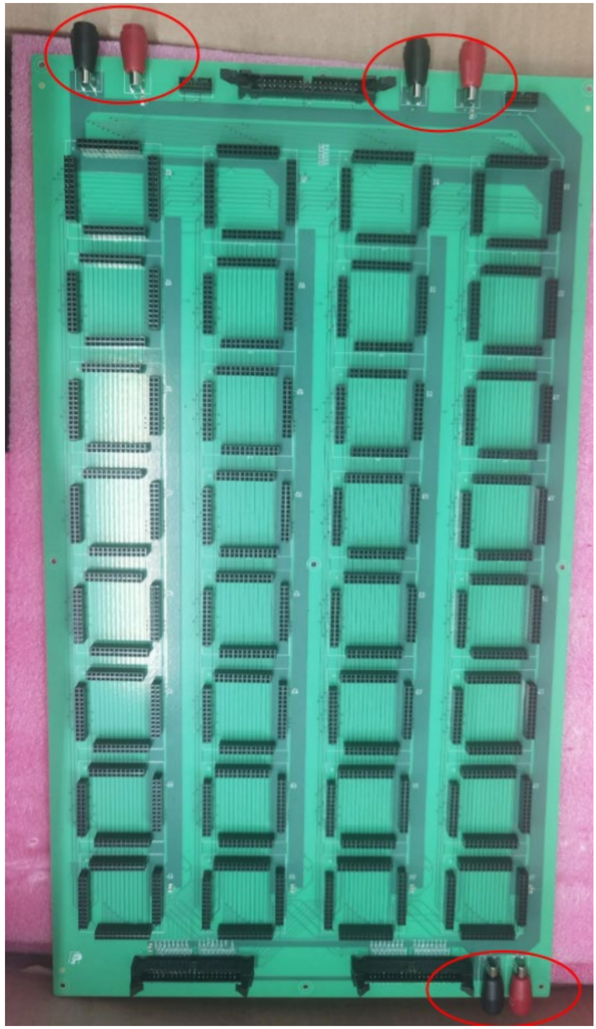


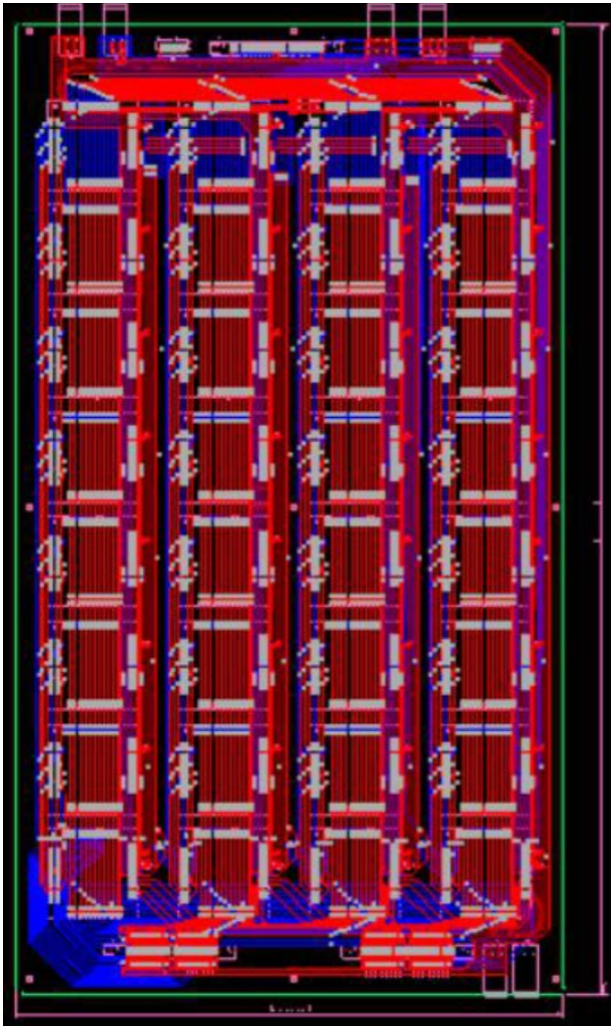
- **Typical on-resistance curve for a QFN88 MUX64 in room temperature**
- **The on-resistances were measured form 0.05V to 1.20V, Step was 0.05V.**
- **All QFN88 MUXs pass the quality assurance test**
    - **64-to-1 function pass**
    - $R_{ON} < 1000\ \Omega$
    - **at room temperature**
- **The QFN88 packaging procedure for MUX64 was validated**

Table 1: **Summary table for MUX64 test**

	wire-bonding test	**QFN-packaged socket test**	**open-cavity test**
Done	12 (Done by Jie)	40 + 84	40

Batch Testing Board





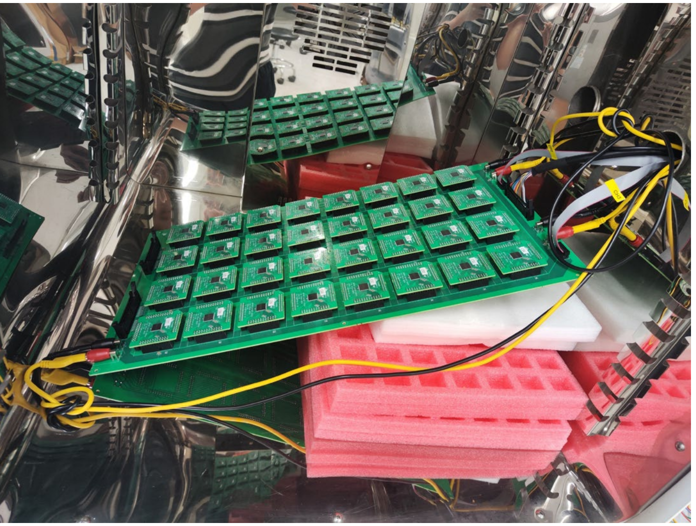
Dimension

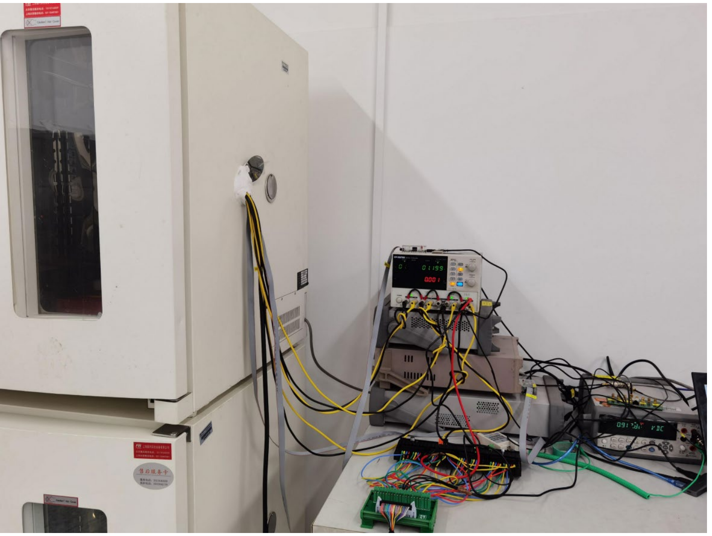
- 292mm×521mm
- Up to 32 MUX64s test on one board

Power supplies

- 1.2V powers the MUX64
- 1.2 powers 64 groups of resistors on the board->Different input voltage for different channels

Reliability Test





Arrhenius acceleration model:

$$AF_T = \exp((E_a/k) \times (1/T_U - 1/T_A))$$

where AF_T is temperature acceleration factor, E_a is activation energy, T_U is operating temperature and T_A is the temperature during acceleration. (set E_a=0.7eV, T_U=25°C, T_A=85°C, k = 8.62E-5 eV/K.)

Average lifespan T:

$$\mathrm{T} = \frac{5 * T.H * AF_T}{\chi^2_{(\%\mathrm{CL},2r+2)}}$$

where $T.H$ is test days, T need more than 5 years (5*365 days). The ratio of twice the total test time to T is chi-squared with r degrees of freedom (get this function through statistics.)

In 60% confidence level, the $\boldsymbol{X^2(\%CL,2r+2)}$=1.83.

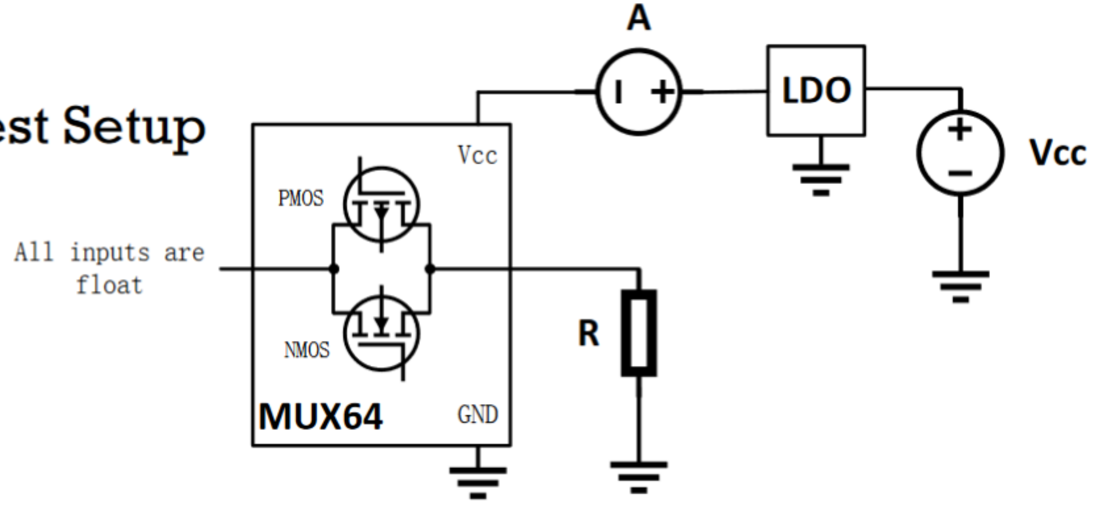
$T.H * AF_T$ =667.95. $AF_T \approx 96$. $T.H \approx 7$ days.

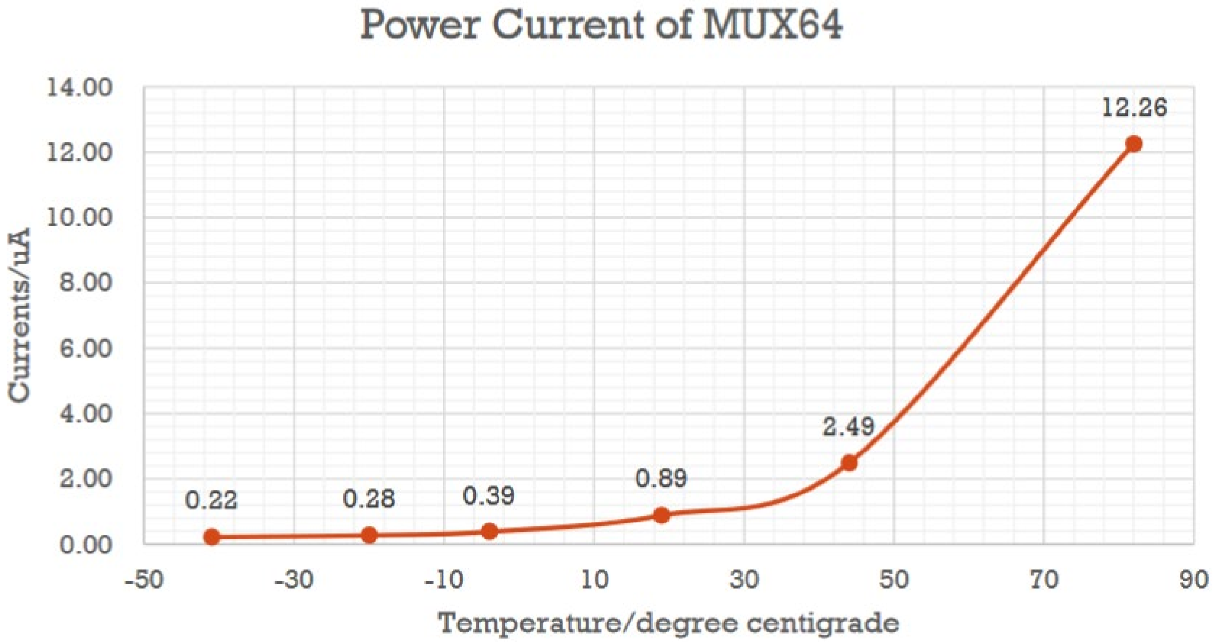
5 years life time requires passing 18 days high temperature reliability test.

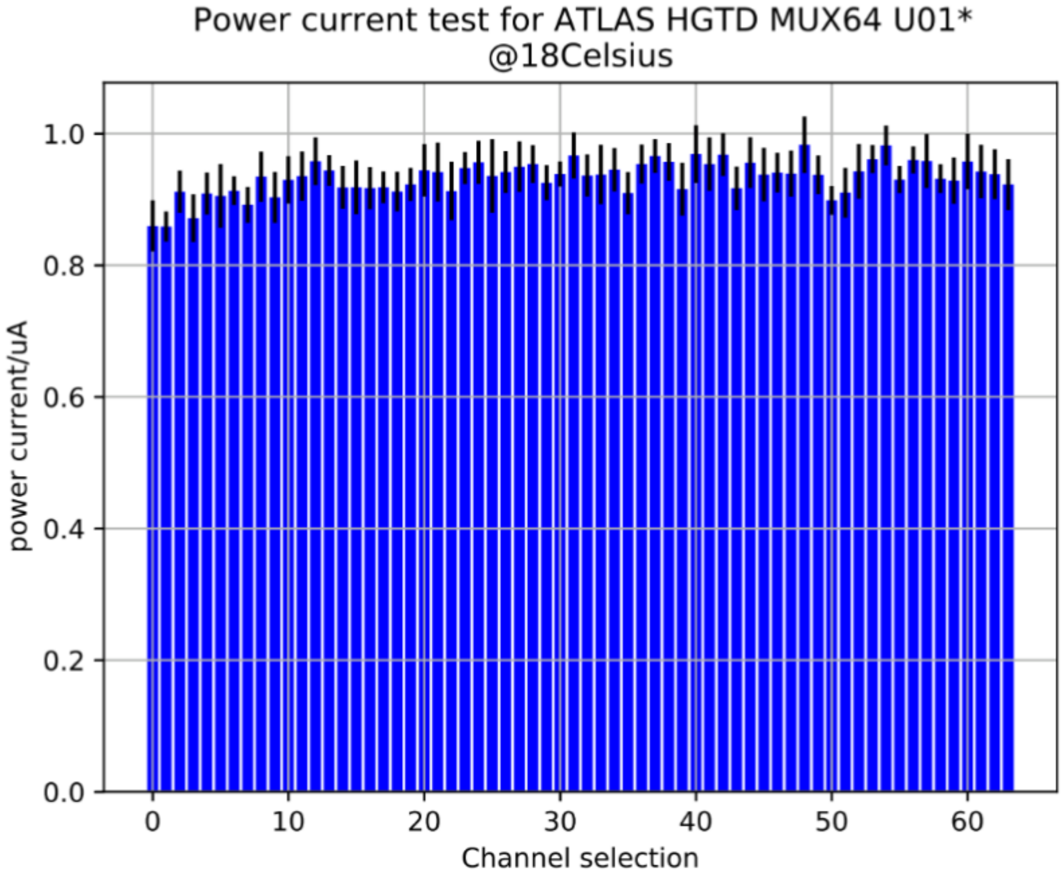
A total 32 MUX64s were tested for ageing effect. The first 16-day aging experiment has been passed, and more aging experiments will continue.

Power Dissipation

- Test Setup







Test power dissipation channel-by-channel

The power dissipation at -20℃ is $0.336\mu W$

Summary for Testing results

The total of 92×3 MUX64 dies in two batches were received in 2021. The chips were tested in both bare-die wire-bonded on PCB and in QFN88 packaged chips. The MUX64 functionality was validated for the input voltage from 0.05 V to 1.20 V. The $R_{\_ON}$ between the selected input channel and the output is measured to be less than 600 Ω at room temperature, which meets the maximum specification range. The $R_{\_ON}$ increased with decreasing temperature, to 1000 Ω at −30 ^{o}C. The power dissipation of MUX64 was 0.336μW@-20°C, which is much less the required 1 mW. All of the chips passed the quality assurance test. A total 32 chips were tested for ageing effect, which demonstrated negligible degradation over 16 days in an 85 ^{o}C burn-in process. The radiation tolerance of MUX64 will be verified in the near future. The full characteristic test results will be presented in the workshop.