TWEPP2022
Topical Workshop on Electronics for Particle Physics,
19th – 23rd September, 2022, Bergen, Norway

MUX64, an analogue 64-to-1 multiplexer ASIC for the ATLAS High Granularity Timing Detector

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Introduction

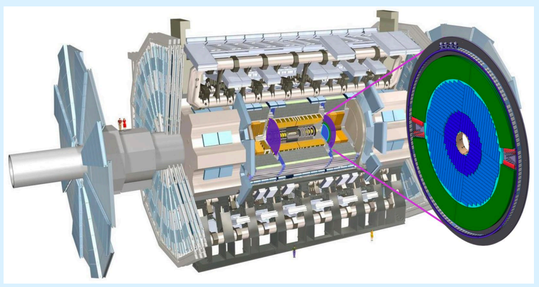

Figure1. Schematic of the ATLAS detector and the HGTD vessel

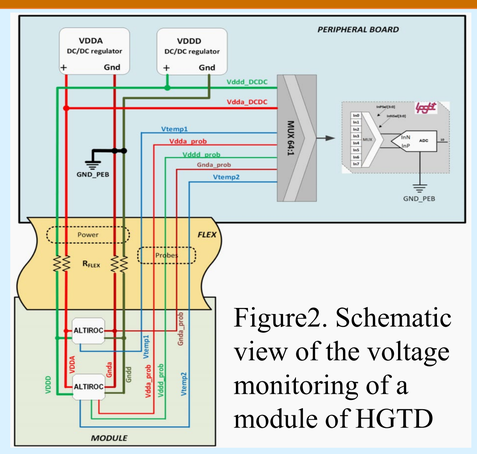

Figure2. Schematic view of the voltage monitoring of a module of HGTD

- The ATLAS High-Granularity Timing Detector (HGTD) [1] for the High-Luminosity LHC upgrade has a monitoring system of detector modules with analogue signals using the ADC channels of the lpGBT chips [2].
- To accommodate the large number of monitoring channels, a multiplexer is implemented for data transfer through a single ADC channel on an lpGBT.
- The MUX64 is a 64-to-1 analogue multiplexer ASIC designed for the HGTD. It transmits one of 64 analogue inputs of voltage or temperature signals to an lpGBT ADC channels through a 6-bit decoder.
- The MUX64 transfers more inputs (up to 64 inputs) than the commercial multiplexers. According to the current TDR estimation, roughly a total of 1300 MUX64 is required in the HGTD.

Chip design

Design Schematic and Function Table

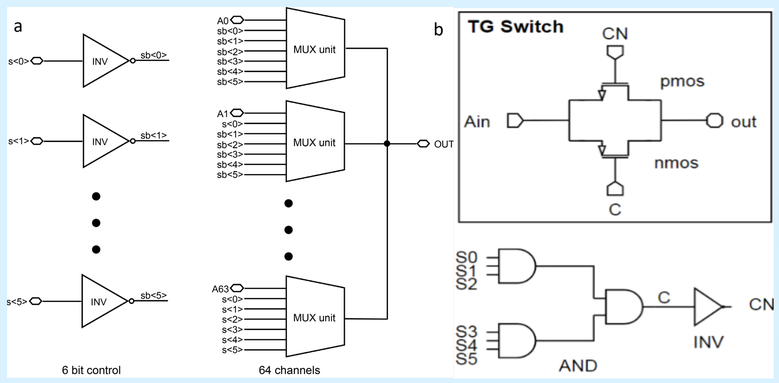

Figure3. a.MUX64 block diagram. b. Schematic of one MUX64 unit. A transmission gate controlled by C and CN

- The MUX64 is designed and manufactured in a TSMC 130 nm CMOS technology.
- The MUX64 die is 2 mm × 2 mm and is packaged in an 88-pin QFN package of 10 mm × 10 mm × 0.75 mm

6-bit addressing

input	s5	s4	s3	s2	s1	s0	out
A0	0	0	0	0	0	0	A0
A1	0	0	0	0	0	1	A1
A2	0	0	0	0	1	0	A2
A3	0	0	0	0	1	1	A3
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
A63	1	1	1	1	1	1	A63

64 analogue inputs

Table1. MUX64 logic function sheet

Design of MUX64

- The MUX64 uses transmission gates to transmit one of the 64 input signals to the output.
- A 6-bit decoder is used to determine which input is connected to the output.

MUX64 Logic Function

- The output is selected by a 6-bit addressing.
- The logic function of MUX64 is exactly the same as a 6-to-64 decoder.

Design Specifications

MUX64 specification	Quantity
Number of inputs	64
Number of output	1
Operates voltage	1.2 V
Dynamic of the input signal	0 ~ 1.0 V
Power dissipation	< 1 mW
R_{ON}	$< 900\ \Omega$
Temperature range	-35~+40 ℃

Table2. Part of MUX64 electrical specifications

	TID [MGy]	NIEL[n_{eq}/cm^2]
ASIC	0.5	1.5×10^{15}

Table3. MUX64 radiation tolerance design requirement [1]

MUX64 Radiation Tolerance

- The radiation tolerance specifications for MUX64 are detailed in the HGTD TDR[1].
- Table4 shows design radiation tolerance of the MUX64 ASIC for operation at the HL-LHC for a total luminosity of 4000 fb^{-1}.

In order to minimize radiation effects

- Enclosed Layout Transistors (ELTs) are employed all over the chip.
- Triple Modular Redundancy (TMR) is implemented in the decoder.

Test result

Technical Progress

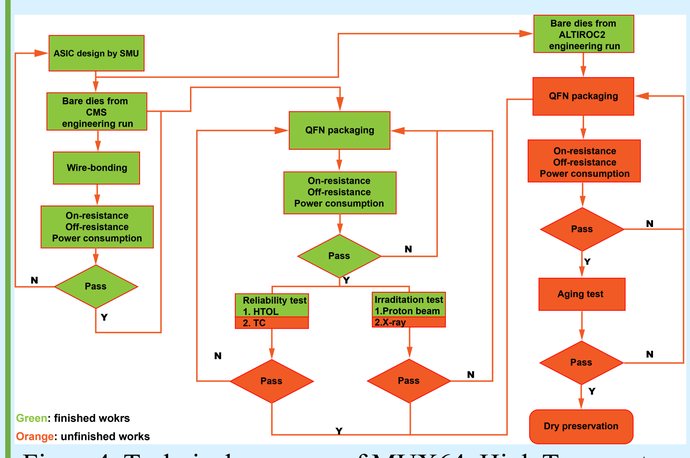

Figure4. Technical progress of MUX64. High Temperature Operating Life(HTOL). Temperature Cycling(TC)

- A total of 92 × 3 dies from CMS engineering run were wire-bonded to PCBs or being packaged chips by QFN88.
- Reliability test and irradiation test are still work in progress.

Test Setup

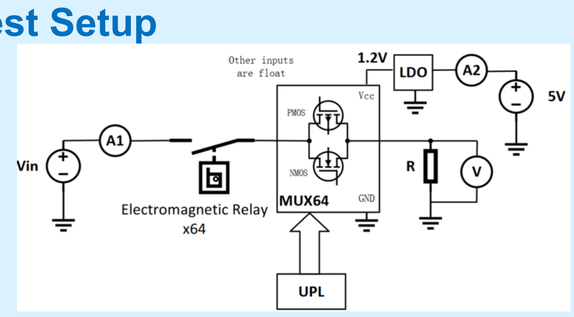

Figure5. Schematic of MUX64 mass production test setup.

Automatic test system

- MUX64 on-channel is selected through a 6-bit address by UPL [3].
- 64 channels input analogue signals selected by a 64-channels relay.

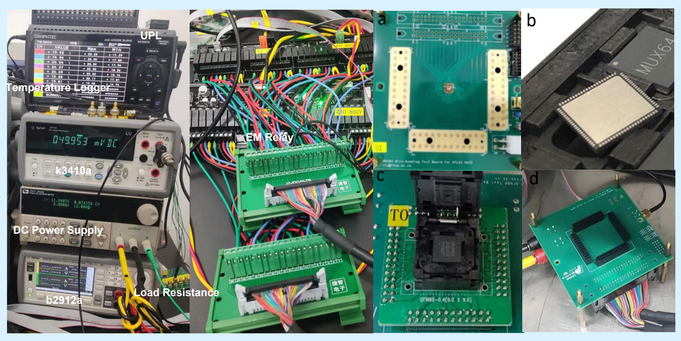

Figure6. Photos of MUX64 test setup. a. Wire-bonded to PCB. b. QFN88 packaged to chips. c. QFN88 packaged MUX64 in a test socket. d. Mass production test PCB

Quality Assurance

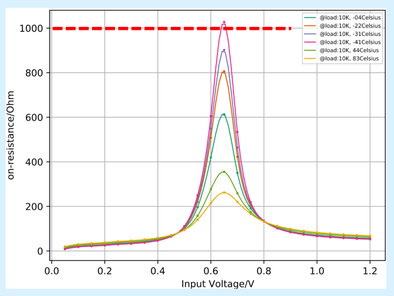

Figure7. On-resistance measurement of a wire-bonded MUX64

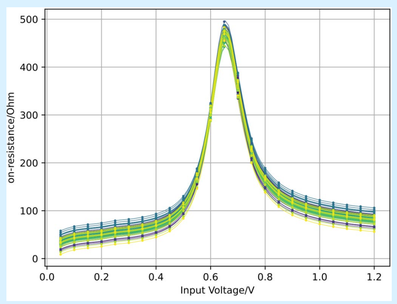

Figure8. One typical on-resistance curve of a QFN packaged MUX64 measured at 20℃

On-resistance measurement at different working temperatures

- Tested temperature range is -41 ~ +85 ℃, larger than the MUX64 design requirement.
- Maximal on-resistance at 0.65 V increases as the temperature decreases.
- On-resistance of the measured MUX64 meets the design demand at -30 ℃.

Batch quality assurance test

- On-resistance dependence of MUX64 is measured from 0.05 V to 1.20 V in steps of 0.05 V.
- A total of 176 pieces were tested. They meet the quality assurance requirement.

Power Consumption

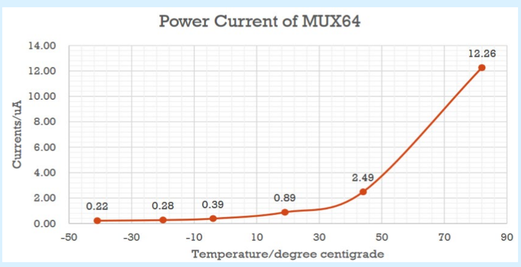

Figure9. Power consumption vs working temperature

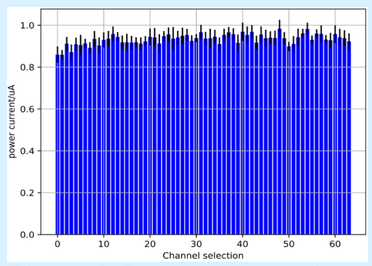

Figure10. Power consumption vs selected channel measured at 18 ℃

- Power consumption at -20 ℃ was 0.336 μW, much less than the design requirement 1 mW.

High Temperature Aging Test

Batch testing PCB

- Up to 32 MUX64 is able to test 64-to-1 function with one board.
- 1.2 V powers the MUX64. 64 different input voltage are integrated on board.

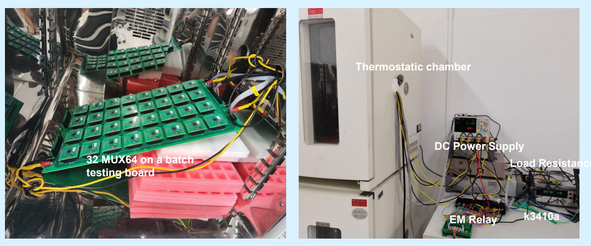

Figure11. Photo of MUX64 reliability test setup

High Temperature Operating Lifetime test result

- 32 MUX64 demonstrated negligible degradation over 16 days burn-in process of 85 ℃.
- According to the Arrhenius acceleration model, lifetime for MUX64 is no less than 4 years at 60% confidence level.
- The largest on-resistance deviation during burn-in $< 5\ \Omega$.

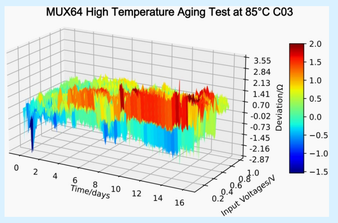

Figure12. One measured on-resistance deviation in 16 days at 85 ℃.

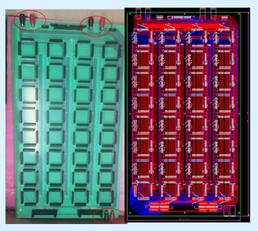

Figure13. Photo and allegro design of the batching testing board

Conclusion and outlook

We present the design and performance of the MUX64. The production bare dies were tested and the results have met design requirements. The burn-in test at 85 ℃ with 32 chips shows negligible degradation over a 16 days period. The Non Ionizing Energy Loss (NIEL) irradiation test has been carried out at a proton beam in CSNS [4]. Two MUX64 chips were tested and sustained the design fluence. Irradiation test in Total Ionizing Dose (TID) is scheduled in later 2022. The quality assurance and thermal cycling durability of all QFN packaged MUX64 chips will be verified.

Acknowledgement: We sincerely thank the Omega group (Omega/Ecole Polytechnique/CNRS, France) for their helpful assistance in the fabrication of the MUX64.

Reference

[1] ATLAS Collaboration, Technical Design Report: A High-Granularity Timing Detector for the ATLAS Phase-II Upgrade, ATLAS-TDR-031.

[2] P. Moreira et al., The lpGBT: a radiation tolerant ASIC for Data, Timing, Trigger and Control Applications in HL-LHC, presented at TWEPP 2019.

[3] L. Han et al., The isolated USB programmer board for lpGBT configuration in ATLAS-HGTD upgrade, presented at TWEPP 2021 ONLINE.

[4] Chen, H., Wang, XL. China's first pulsed neutron source. *Nature Mater* **15**, 689–691 (2016). https://doi.org/10.1038/nmat4655