Contribution ID: **160** Type: **Poster**

MUX64, an analogue 64-to-1 multiplexer ASIC for the ATLAS High Granularity Timing Detector

Thursday, 22 September 2022 16:40 (20 minutes)

Abstract:
We present the design and the performance of MUX64, a 64-to-1 analogue multiplexer ASIC for the ATLAS High Granularity Timing Detector (HGTD). The MUX64 transmits one of its 64 inputs of voltages or temperatures to an lpGBT ADC channel through a 6-bit decoder. A total of 92x3 dies were fabricated in two batches by the TSMC 130 nm CMOS technology. All of them passed the quality assurance test after bare dies were wire-bonded to PCBs or being packaged chips. Negligible degradation was observed in a 16-day aging test at 85℃.

Summary (500 words)

In the ATLAS High-Granularity Timing Detector (HGTD) for the High-Luminosity LHC upgrade, it is important to monitor the temperature of the Low-Gain Avalanche Detectors (LGAD) sensors and the supply voltage drops in flex cables. These analogue signals are monitored with the ADC channels of the lpGBT chips, mounted on the Peripheral Electronics Boards (PEBs). Each lpGBT has only 8 ADC input channels. To accommodate the large number of monitoring channels of temperatures and voltages required for the LGAD sensors, the multiplexer is required to be interfaced to a single ADC channel on an lpGBT. A multiplexer must have 64 analogue inputs and a single analogue output. The dynamic range of input analogue signals is from 0 to 1.0V. To achieve the required resolution, the on-resistance (R_ON) between the selected input channel and the output must be lower than 900 Ω. The operating temperature range for the multiplexer is -35℃ to + 40℃. The power dissipation must be less than 1 mW.

MUX64, a 64-to-1 analogue multiplexer ASIC, has been developed. The MUX64 uses transmission gates to transmit only one of the 64 input signals to the output. The MUX64 has a 6-bit decoder to determine which input channel is connected to its output. To minimize radiation effects, Enclosed Layout Transistors (ELTs) are employed all over the chip and Triple Modular Redundancy (TMR) is implemented in the decoder. The MUX64 is designed and manufactured in a TSMC 130 nm CMOS technology. The MUX64 operates in a single voltage of 1.2 V. The dimension of MUX64 die is 2 mm x 2 mm and is packaged in an 88-pin QFN package of 10 mm × 10 mm × 0.75 mm.

A total of 92×3 MUX64 dies in two batches have been fabricated and preliminarily evaluated. The chips were tested in both wire-bonding bare-die on PCB and in QFN88 packaged. The MUX64 functionality was validated for the input voltage from 0.05 V to 1.20 V. The on-resistance (R_ON) is measured to be less than 600 Ω at room temperature, which is better than the maximum specification range. The on-resistance increased with decreasing temperature, to 1000 Ω at -30℃. The power dissipation of MUX64 was 0.336μW at -20℃, which is much less the required 1 mW. All of the chips passed the quality assurance test. A total 32 chips were tested for ageing effect, which demonstrated negligible degradation over 16 days in a burn-in process of 85℃. The radiation tolerance of the MUX64 ASIC chips will be verified in the near future. The full characteristic test results will be presented in detail at the workshop.

Primary authors: Mr XU, Zifeng (Nanjing University (CN)); ZHANG, Li (Southern Methodist University); HUANG, Xing (Southern Methodist University); SHA, Qiyu (Chinese Academy of Sciences (CN)); GE, Zhenwu (Nanjing University (CN)); CHE, Yimin (Nanjing University (CN)); GONG, Datao (SMU); HOU, Suen (Academia Sinica); ZHANG, Jie (Institute of High Energy Physics(IHEP), Chinese Academy of Sciences(CAS)); LIU, Tiankuan (Southern Methodist University (US)); LIANG, Zhijun (Chinese Academy of Sciences (CN)); ZHANG, Lei (Nanjing University (CN)); YE, Jingbo (Southern Methodist University); QI, Ming (Nanjing University (CN))

Presenter: Mr XU, Zifeng (Nanjing University (CN))

Session Classification: Thursday posters session

Track Classification: ASIC