Contribution ID: **169** Type: **Poster**

CIC a radiation tolerant 65nm data aggregation ASIC for the future CMS tracking detector at LHC

Tuesday 20 September 2022 16:40 (20 minutes)

The Concentrator Integrated Circuit (CIC) ASIC is a front-end chip for both Pixel-Strip (PS) and Strip-Strip (2S) modules of the future Phase-II CMS Outer Tracker upgrade at the High-Luminosity LHC (HL-LHC). This data aggregator, designed in 65nm CMOS technology, will be a key element of the tracker front-end chain. Two versions, CIC1 and CIC2, were tested successfully in 2019 and 2021 respectively. The design, implementation, and preliminary test results of the final version, CIC2.1, are presented.

Summary (500 words)

The Concentrator Integrated Circuit (CIC) ASIC is a front-end (FE) chip for both Pixel-Strip (PS) and Strip-Strip (2S) modules of the future Phase-2 CMS Outer Tracker (OT) upgrade at the High-Luminosity LHC (HL-LHC). This 65nm CMOS radiation tolerant data aggregator is a fundamental element on the future detector FE chain.

The main OT feature will be its inclusion at the first level of the CMS trigger system. 40MHz readout of the detector is therefore necessary. To this end, a very innovative detection element, the pT-module, has been developed. The main principle, two silicon layers separated by a few mm, is relatively standard in current tracking systems. Readout electronics, on the other hand, is entirely original. Indeed, for the first time, the signal of the 2 layers will be put in coincidence directly at the module level, thus allowing
a significant reduction of the detector output data rate. This coincidence will be performed by a set of 3 very front-end ASICs types: CBC and SSA/MPA for 2S and PS modules respectively. Each pT-module will contain 16 such ASICs, each of them handling the readout of around 120 detection channels.

The CIC handles the data produced by those chips and performs another data compression stage. It receives different input streams from 8 FE chips, either MPAs or CBCs (there are 2 CICs per module), processes them, and finally sends out a standardized data stream to one lpGBT ASIC which transmits the data of both CICs. In average the CIC reduces the data throughput by an order of magnitude. It has to be compatible with both module flavors (different hybrids, voltages, input streams) and his therefore highly configurable.

Two first version of the CIC were previously developed and tested: CIC1 in 2019 and CIC2 in 2020. CIC1 was a first test vehicle incorporating most of the functionalities of the final system except the radiation hardness and the 640MHz output capability. Those features were included in CIC2. Successful characterizations campaigns led to the development of the final chip version: CIC2.1, which was produced and tested in 2022.

Author: NODARI, Benedetta (Centre National de la Recherche Scientifique (FR))

Co-authors: VIRET, Sebastien (Centre National de la Recherche Scientifique (FR)); CAPONETTO, Luigi (Centre National de la Recherche Scientifique (FR)); SCARFI', Simone (CERN); GALBIT, Geoffrey Christian (Centre National de la Recherche Scientifique (FR))

Presenter: NODARI, Benedetta (Centre National de la Recherche Scientifique (FR))

Session Classification: Tuesday posters session

Track Classification: ASIC