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RISC-V processor evaluation with Cadence Protium platform

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RISC-V is an open standard instruction set architecture with a large community that gives access to many resources (such as architecture, operating systems, tool chains, ...). The use of such a processor could be interesting in several ways for the HEP community. For example, it could be used to have a versatile supervisor of complex chips. The purpose of this presentation is to evaluate the development of RISC-V using the Protium prototyping platform from Cadence. Protium is an FPGA board based solution for prototyping digital ASICs without any RTL modifications.

Summary (500 words)

The large community around the RISC-V open-source standard makes it an ideal candidate for integration of a processor in an ASIC. Such integration is not very common in the HEP community. The operating environment (radiation, low power ...) as well as the use of old technology nodes are obstacles to their use. However, the availability of open hardware solutions allowing their adaptation to our environment and the recent developments in finer nodes allows us to foresee their appearance in front-end ASIC or MAPS. At first, they will probably not be used for computation because of the power consumption, but they can be used as programmable supervisors for more and more complex ASICs. It is in this context that we decided to study the development of a RISC-V processor and the possibilities that can be offered. For example, the supervisor can be programmed to calibrate automatically the pixels of a MAPS, since this operation need several loops to configure a large number of registers. These configurations use many slowcontrol transactions which are time consuming. We chose the pulpissimo platform because of its very open nature [1].
The processor evaluation is performed on Cadence's prototyping solution called Protium S1. It uses a large FPGA (Xilinx Ultrascale VU440) and has a dedicated software to implement RTL code adapted to ASICs with only a few modifications. Indeed, the RTL code realized for ASICs could not be implemented directly in FPGAs and requires specific developments. These developments are time consuming and can lead to non-visible bugs. Since the processor is integrated in the prototyping platform, it is possible to run the software or firmware directly on it. The signals can be probed by Vivado for debugging purposes. The development time is reduced compared to that based on simulations since the processor runs on the FPGA at a few MHz. The processor runs at a lower speed than the direct FPGA implementation because of the environment provided by Cadence to run the RTL code without modifications. In the case of developing specific hardware processing engines, prototyping facilitates co-development of the hardware, software and tool chain. The hardware implementation can be validated even before the foundry.

[1] Pasquale Davide Sciavone and al. "Quentin: an Ultra-Low-Power PULPissimo SoC in 22nm FDX", 2018 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)

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