Fast Tracking Read-Out Electronics for ATLAS sMDT Detectors in 65nm CMOS

Abstract:

This paper presents 4-channel readout electronics for small-diameter Muon-Drift-Tube (sMDT) detectors. Design is optimized largely for higher detection rate of events at High Luminosity of LHC and thus significantly reducing the impact of pile-up events and eliminating use of long deadtime zone. Analog chain of the design consists of Charge-Sensitive-Preamplifier, to convert input charge into voltage pulse, followed by a shaper. Novelty of design is in fast resetting all stages just after the charge information is extracted. Design operates with a 5 –100 fC input charge range. The design is realized in 65nm technology and operated is from 1.2V supply.

Summary:

For Phase-2, LHC is under an aggressive improving process and is expected to be operated at a very high luminosity, increasing by a factor of seven as compared to its previous performance, to discover novel physics particles. These advancements at LHC create further challenges and demand more efficient read-out electronics to detect charges at higher data-rate. Currently, the Muon Drift Tubes (MDT) chambers of ATLAS experiment utilize read-out electronics (known as ASD, Amplifier-Shaper-Discriminator) which are based on Bipolar shaping scheme of input pulse. One of the major problems with these systems is multiple hits on signal-tail of the bipolar signal and hence are not detected due to dead-time of the circuit, nominally set to 500 ns, resultantly decreasing the efficiency of detecting charges. For this reason, the presented read-out electronics design, implements an efficient reset technique to enhance detection efficiency of the system. Rather than waiting the complete output of the shaper the device is reset as soon as the useful information is extracted from the incoming pulse and the readout electronics are ready to detect any new incoming charge pulse. It is a mixed signal design comprising of an analog and digital section. The analog section consists of a dedicated CSP followed by a Shaper. The CSP is designed with a two-stage differential amplifier with a feedback network of a resistor and capacitor in parallel. A switch is used in this feedback path and also in parallel with the miller-capacitor to perform the reset operation, when activated. The shaper stage is also designed using a two-stage differential topology and is operated in sub-threshold region. To set the common mode voltage a common-mode feedback (CMFB) network has been designed, connected through a sensing network to the main amplifier. The shaper amplifies and shape the voltage signal generated by the CSP. The Analog section is followed by two comparators to perform A-D (Analog to Digital) conversion. Both the comparators are designed using un-compensated, two-stage differential topology followed by a series of inverters. Thresholds for the comparators are programmed externally and the RESET signal is generated by output of the comparators. However, at any time, the signal processing in the channel can be overdriven by the external reset. Utilizing two threshold-voltage crossing, for every incoming charge pulse, the system gives information about charge arrival-time and the amount of charge been detected utilizing ToT (Time-over-Threshold) encoding. The design is capable of detecting charge in range of 5 -100 fC.

Test point buffers, designed using a common drain amplifier topology, are connected at the output of CSP and Shaper for monitoring purpose while measurement.

Conclusions

4-channels readout electronics for small-diameter Muon Drift-Tube has been presented. The design has been realized in TSMC 65nm Technology. The total area of the design is 4 mm^2. Due to the use of efficient reset-scheme the efficiency of detecting charges at high hit rate has been improved and the use of dead-time logic has been eliminated.

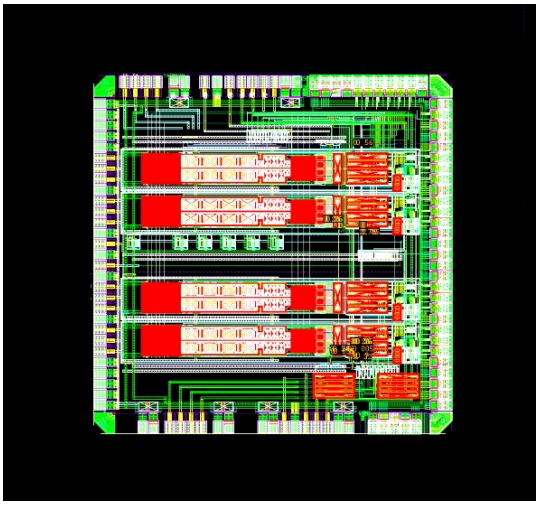

Figure 1 Four-channel Readout Electronics design layout.

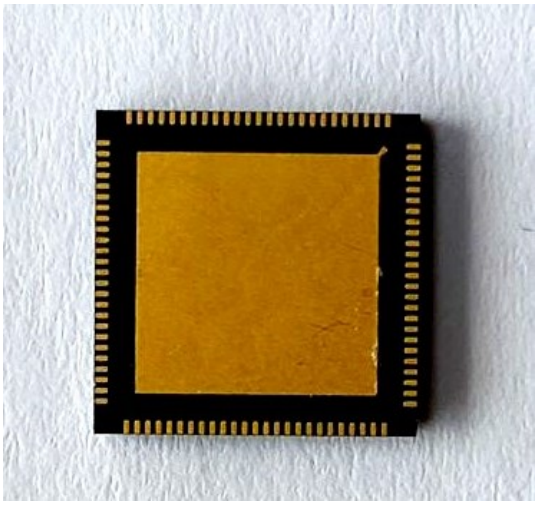

*Figure 2 Chip placed in QFN-100 12mm * 12mm package*