Contribution ID: **67** Type: **Oral**

DART28-FPGA implementation study for future high-speed links

Wednesday 21 September 2022 09:00 (20 minutes)

The data link from the detectors to the back-end stage must keep up with the requirements from the upcoming generation of High Energy Physics experiments. Pushing the limit of the Non-Return-to-Zero (NRZ) modulated signals, a line rate of up to 28 Gbps can be realized. In this talk, the implementation of the DART28 demonstrator system based on FPGA platforms from Xilinx and Intel will be presented. The performance characteristic of these links will be discussed, and the Forward Error Correction (FEC) performance will be compared to that of an ideal model.

Summary (500 words)

The data link from the detectors to the back-end stage must keep up with the requirements from the upcoming generation of High Energy Physics experiments. Last year, we presented at TWEPP the investigation on the feasibility and limitation of high data-rate links based on the PAM-4 technology. PAM-4 poses strict constraints on the data-rate of links which translates into a highly complex rad-hard SerDes design. Alternatively, pushing the limit of the Non-Return-to-Zero (NRZ) modulated signals, a line rate of up to 28 Gbps can be realized. This is less constraining thanks to the possibility of bypassing retimers of NRZ modules.
As a part of the Work Package 6 of the CERN EP Research and Development programme, the feasibility as well as the availability in the telecom and datacom market of such NRZ links have been investigated. The rate of 25.6 Gbps per lane (an integer multiple 640 of the 40MHz Bunch Clock) with NRZ modulation have been identified as the target for the next generation of detector-to-backend links. The DART28 chip, designed at 28nm and targeting high-radiation hardness, is currently being designed at this data-rate with a custom protocol and a Reed-Solomon Forward Error Correction (FEC).
A proof-of-concept on FPGA emulating the DART28 protocol has been built for early evaluation. The system uses commercially available optoelectronics transceiver and FPGA platforms to implement the DART28 datapath containing a scrambler, interleaving and FEC. The VCU129 Xilinx Virtex Ultrascale+ and Intel Stratix 10 evaluation boards were used for this work. In this talk, the implementation of the demonstrator systems will be presented. The performance characteristic of these links will be discussed and the FEC performance will be compared to that of an ideal model.

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Session Classification: Programmable Logic, Design Tools and Methods

Track Classification: Programmable Logic, Design Tools and Methods