An FPGA-based readout chip emulator for the CMS ETL detector upgrade

1. Introduction

An Endcap Timing Read-Out Chip (ETROC) is being developed for the CMS MIP Timing Detector (MTD) [1]. Two prototypes, ETROC0 [2] and ETROC1 [3], have been designed and tested. ETROC0 consists of a pre-amplifier and a discriminator. ETROC1 implements a standalone Time-to-Digital Converter (TDC) [4], a single-pixel full-chain readout circuit, and the readout circuit of a 4x4 pixel array. The third prototype, ETROC2 [5], will be submitted in mid-2022. The block diagram of ETROC2 is shown on the left side of figure 1. ETROC2 includes an array of 16×16 pixels located on the top of the chip, and a global readout logic located on the bottom of the chip. Each pixel has a Trans-Impedance Amplifier (pre-amplifier), a discriminator whose threshold can be programmed with a Digital-to-Analog Converter (DAC), a TDC, and buffers. The global readout logic has a Phase-Locked Loop (PLL), a fast command decoder, a digital readout logic, and an I2C target module. Each ETROC2 receives a 40 MHz clock (CLK40) and a 320 Mbps Fast Command (FC). ETROC2 sends its left and right digital outputs (DOL and DOR) at a data rate of 320 Mbps, 640 Mbps, or 1.28 Gbps.

The ETL readout system is shown on the right side of figure 1. Multiple ETROCs are connected to a readout board. Each readout board consists of a VTRx+ module, two lpGBT chips, and a GBT SCA. The VTRx+ module communicates with the off-detector Data Acquisition (DAQ) board via optical fibers. The first lpGBT recovers clocks and fast commands from a downstream link for the ETROCs, while both lpGBT chips transmit the data from ETROCs to the DAQ board through two upstream optical links. The GBT SCA provides slow control of the ETROCs. A power mezzanine board is mounted to the readout board to provide supply voltages.

To decouple the system development from the ETROC development before ETROC2 is available and to verify the digital readout scheme, an FPGA-based ETROC emulator board is developed. The emulator board has the same electrical interface, including I/O pins, the fast command definition, and the output data frame definition, as ETROC2. Each emulator board emulates the functions of four ETROC2 chips.

2. Hardware design

The block diagram of the ETROC emulator is shown on the left side of figure 2. The functions of ETROC to be emulated include a PLL, a fast command decoder, an I2C target, and a readout logic. The PLL generates internal clocks from the input 40 MHz clock. The command decoder recovers fast commands from the command bitstream. The I2C target communicates with the I2C

controller. The data generator generates data in each clock period of 40 MHz, stores them into a circular buffer, and transfers them to an L1A event buffer when an L1A command is asserted. Then the trigger selected data are read out in specific order to a global data stream buffer and transmitted out of the FPGA in a framed format. When no data are available, frame fillers are transmitted. To ease the firmware test, we also emulate the counterparts located on the readout board and the DAQ board. To generate four clock outputs, we use a clock fanout chip (part number CDCLVD1208 produced by Texas Instruments). We use two cables to connect the ETROC emulator board to the readout board. The first cable is a 6" 34AWG Twinax cable with 12 differential pairs. The other cable is a 24-pin flat ribbon cable for power and slow control signals. The emulator requires a single 12 V voltage with a current of about 0.5 A. All the supply voltages are generated through DC-DC converters or Low-Drop-Out (LDO) regulators. The emulator has passive loads for the readout board to monitor supply currents.

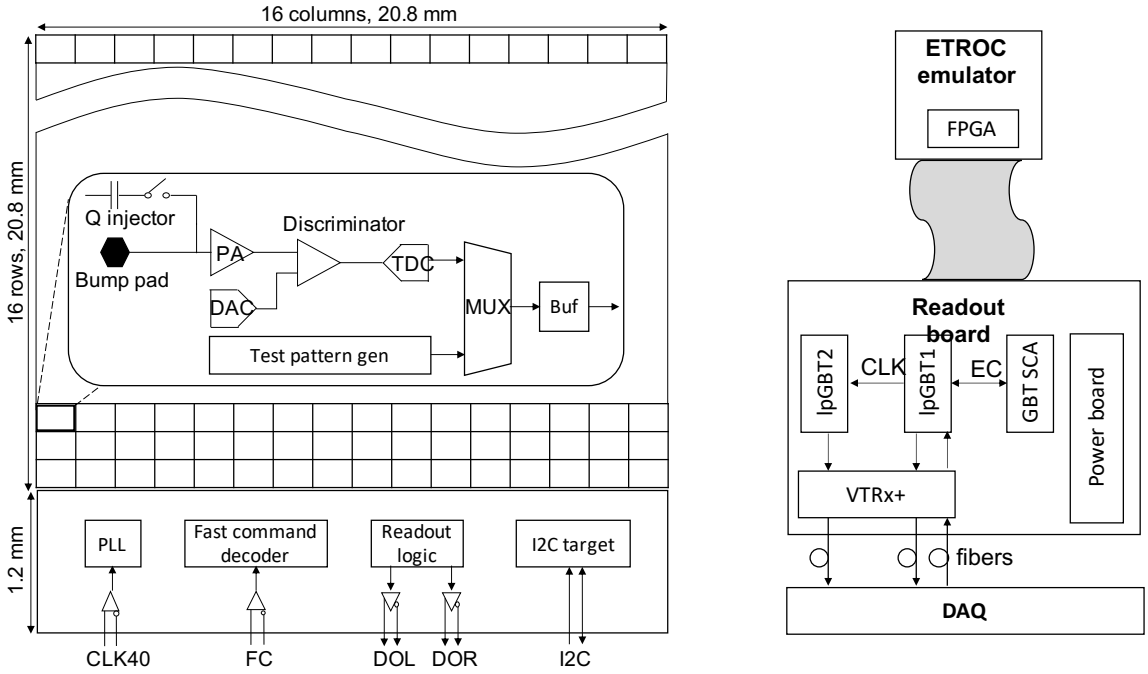

Figure 1. Block diagram of the ETROC2 (left) and the ETL readout system (right).

Considering the logic compatibility and the data rate range of general-purpose I/Os pins, we select an Intel Cyclone 10 GX FPGA (Part number 10CX220YF780E5G). For the ETROC emulator, all differential input signals are in LVDS standard, while all differential output signals are in differential SSTL-12 standard. All I2C signals are in the 1.2 V LVCMOS standard. These logic levels are compatible with lpGBT and GBT SCA. The FPGA has five high-performance I/O banks that support 1.2 V LCCMOS logic and differential 1.2 V SSTL logic and a high-range I/O bank that supports a VCCIO of 1.8 V or higher. We use four high-performance I/O banks to emulate the functions of four ETROC chips, while the fifth high-performance I/O bank to emulate the readout board for loopback tests. The high-range I/O bank is used for a JTAG interface and a flash memory.

The ETROC emulator has 10 layers and is 165 mm long and 43 mm wide. The width of the emulator matches that of the ETROC modules. A photograph of an emulator with loopback cables plugged is shown on the right side of figure 2.

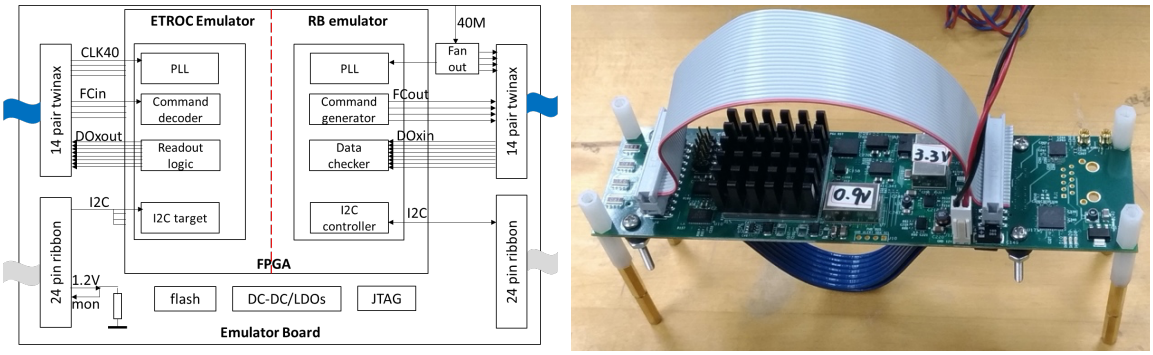

Figure 2. Block diagram of the EETROC emulator (left) and photograph of an Emulator board with cables plugged for loopback tests.

3. Firmware development

Based on the actual ETROC design, the firmware is being developed and verified on the emulator board. As discussed before, the ETROC emulator implements a fast command decoder, a digital readout logic, and an I2C target. To ease loopback tests, the emulator also implements the counterparts on the readout/DAQ board side, including a fast command generator, a data checker, and an I2C controller.

The fast command decoder searches for the command boundary and recovers commands from the serial bitstream. The data rate of the fast command bitstream is 320 Mbps, so each fast command has eight bits. The following tentative fast commands have been implemented. Idle is a command when no other command is sent and can be used for fast command alignment. Bunch Crossing Reset (BCR) resets the internal counter, whose value serves as the Bunch Crossing Identification (BCID). The BCID increases at every bunch crossing clock of 40 MHz from 0 and rounds automatically from a user-configurable integer (by default 3563) back to 0 even if no BCR is asserted. Level-1 Acceptance (L1A) indicates the corresponding event is accepted by the trigger system. L1A & BCR is the combination of L1A and BCR. L1A-CR resets the internal L1A counter of ETROC to 0. Charge Injection enables the charge injection circuits for calibration purposes. Fast commands are encoded in a Hamming code with a minimum distance of 3 bits between any two commands. Any single bit flip, for example, a radiation-induced Single Event Upset, can be corrected. The fast command decoder has been verified in the loopback test.

The digital readout logic is the core of firmware development. The block diagram of the digital readout logic is shown in figure 3. ETROC has 16x16 pixels or channels. For each channel, the data are generated either from a Time-to-Digital Converter (TDC) or a test pattern generator. In a TDC, the Time of Arrival, the Time Over Threshold, and a Calibration code are measured, as well

as a Dada Valid bit indicating if the pixel is hit. The pixel data are stored in a circular buffer at every bunch crossing. Once an L1A is asserted, the corresponding data stored in the circular buffer are transferred to an L1A event buffer. A switching network transmits the trigger-selected data of all channels to a global data stream buffer. The order of data transferring depends on the position of the pixel. The data in the global data stream buffer are encoded into frames and serialized into a serial bitstream. On the receiver side, the serial bit stream is deserialized. After the frame boundary is identified, the data are extracted and checked. The deserializer, the data extractor, and the data checker are implemented for loopback tests.

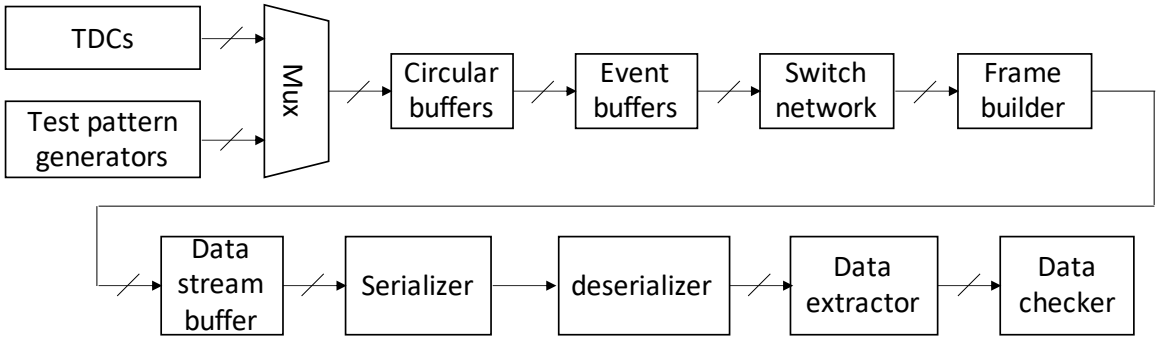

Figure 3. Block diagram of readout logic.

The whole switching network in ETROC2 is shown on the left side of figure 4. Each pixel has an event buffer and a switching cell. The switching cell has its own data (marked as a red arrow) and two neighbors (upstream marked as a blue arrow and downstream marked as a green arrow). The 16 pixels in a column form a column chain. In a column chain, the pixel on the bottom has the highest priority to transmit its data, whereas the pixel on the top has the lowest priority. At the bottom of columns, 15 extra switching cells form a row chain and connect the 16 columns to the global data stream buffer. In the row chain, the pixel on the left of the center has the highest priority and the pixel on the rightmost has the lowest priority.

The switching cell is a combinational logic circuit that controls the data transmission from multiple event buffers to the global data stream buffer. A pixel transmits its data before its upstream neighbor if it is not empty. The data pass the pixels with empty data, and propagate downstream, while the control signals propagate in the opposite direction. The schematic of a switching cell is shown on the right side of Figure 4. Each pixel has a Data Valid (DV) flag to indicate if the pixel is hit. At the beginning of reading out an event, a load (LD) pulse is sent so that the DV signal is passed to DVA. The data is written from DY to the global data stream buffer and CLRY is set in the same clock cycle. Then DVA is cleared and the data from upstream channels are fed from DB and passed to DY. Only one pixel is processed within a bunch crossing clock cycle.

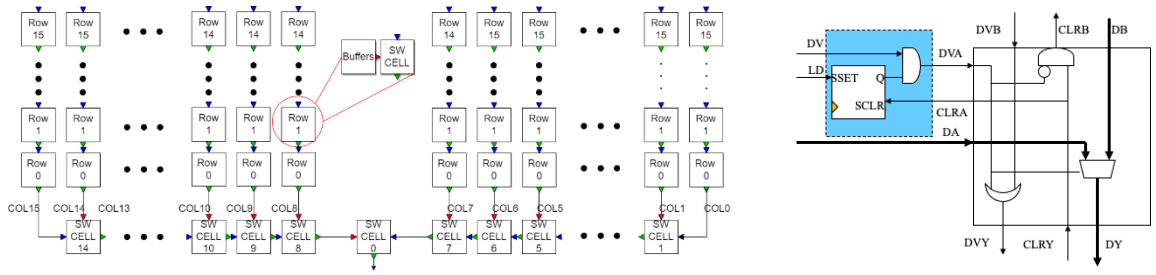

Figure 4. Block diagram of the switching network and schematic of a switching cell.

The data from the data stream buffer are framed and serialized as a serial bitstream. We proposed and implemented a tentative frame format with a fixed length of 40 bits. The serial output data are the combination of four different types (headers, pixel data, trailers, and fillers) of frames. Every event has a header, data frames of multiple pixels that are hit, and a trailer. If no data are transmitted (no L1A), a filler is transmitted. The frame format has been verified to be capable of recovering the frame boundary reliably.

4. Verification and applications in system tests

The emulator board is being used for the ETROC digital design verification as well as for the system development before ETROC is available. The ETROC emulator has been verified with one single emulator board and loopback cables. Figure 5 is a screenshot of a logic analyzer (Signal Tap II). Only one frame with two hit pixels is displayed. A trailer of the previous event precedes the frame with a header, the data of two pixels, and a trailer. The frame is followed by a filler. The screenshot also includes a lot of test signals, which will not be described in detail.

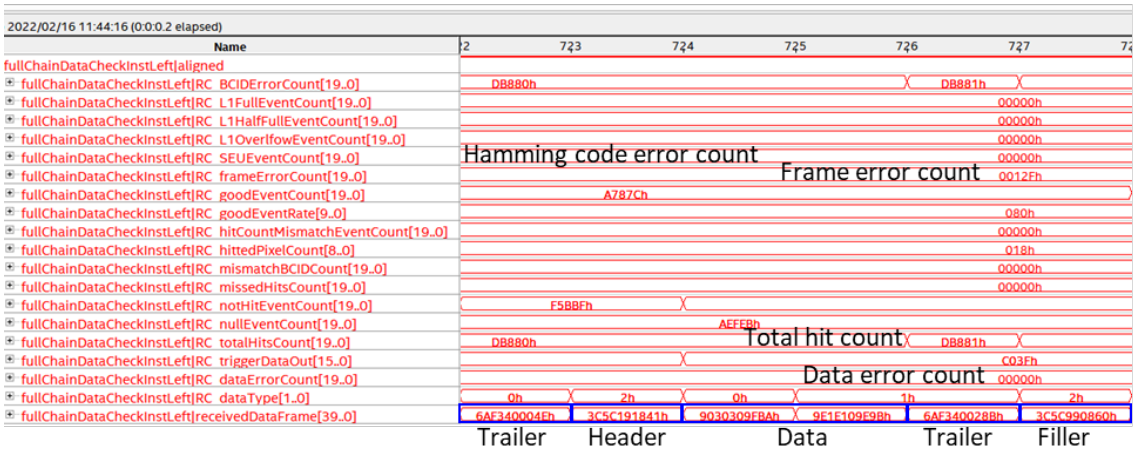

Figure 5. ETROC data simulation waveforms.

The emulator has been verified with two connected emulator boards. Emulator 1 received an external 40 MHz clock, fanned out the clock, and encoded fast commands. Emulator 2 generated test patterns and sent the data back to Emulator 1, based on the clock and fast command received from Emulator 1. Emulator 1 also checked the data generated in Emulator 2. The test system has

been running for a whole day without any data format errors.

The emulator board is being used in the system test of the readout board. In the test, a readout board communicated with three emulator boards and an FPGA evaluation board Xilinx KCU105, which serves as the DAQ board. Preliminary results indicate that the data generated by the emulators can be extracted successfully.

5. Conclusion

An FPGA-based ETROC emulator has been developed for the CMS Endcap Timing Layer (ETL) detector upgrade. The emulator board uses an Intel Cyclone 10 GX FPGA to emulate the functions of four Endcap Layer Readout Chips (ETROCs), each including a PLL, a fast command decoder, a digital readout logic, and an I2C target. Based on the actual ETROC design, the firmware is implemented and preliminarily verified. The emulator board is being used for the ETROC digital design verification as well as for the system development before ETROC is available.

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References

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