Contribution ID: **155**   Type: **Oral**

An FPGA-based readout chip emulator for the CMS ETL detector upgrade

Wednesday 21 September 2022 11:40 (20 minutes)

We present an FPGA-based readout chip emulator board for the CMS Endcap Timing Layer (ETL) detector upgrade. The emulator board uses an Intel Cyclone 10 GX FPGA to emulate the functions of four Endcap Layer Readout Chips (ETROCs), each including a PLL, a fast command decoder, the pixel and global data readout, and an I2C target. Based on the actual ETROC design, the firmware is implemented and preliminarily verified. The emulator board is being used for the ETROC digital design verification as well as for the system development before ETROC is available.

Summary (500 words)

ETROC is an Endcap Timing Read-Out Chip that is being developed for the CMS MIP Timing Detector (MTD). Two prototypes, ETROC0 and ETROC1, have been designed and tested. The third prototype, ETROC2, which includes an array of 16⊠16 pixels and a full-chain digital readout logic, will be submitted in mid-2022. To decouple the system development from the ETROC development before ETROC2 is available and to verify the digital readout scheme, an FPGA-based ETROC emulator board is developed.

```
The emulator board is a 10-layer printer circuit board. The board is 165 mm long and 43 mm wide. The board impler
```

Based on the actual ETROC design, the firmware is implemented and preliminarily verified. The tentative fast commands, including command alignment idle, Bunch Crossing Reset (BCR), Level-1 Acceptance (L1A), L1A & BCR, Link Reset, charge injection enable, BCR & L1A, and L1A & event Counter Reset (CR), have been proposed, implemented, and verified in the loopback tests on the emulator board.

A full-chain digital readout logic has been implements and verified in the emulator loopback tests. For each pixel, the Time of Arrival, the Time Over Threshold, and a Calibration code, which are measured in a Time-to-Digital Converter (TDC), as well as a flag bit indicating that the pixel is hit, are stored in a circular buffer at every bunch crossing. Once an L1A is asserted, corresponding data stored in the circular buffer are transferred to a data stream buffer through a switching network. The data in the global buffer are encoded into frames and serialized into a serial bitstream. A tentative frame format with a fixed frame length of 40 bits has been proposed and implemented. On the receiver side, the serial bit stream is deserialized. After the frame boundary is identified, the data are extracted and checked. The deserializer, the data extractor, and the data checker are implemented for loopback tests.

The emulator board is being used for the ETROC digital design verification as well as for the system development before ETROC is available. The ETROC emulator has been verified with one single emulator board and loopback cables or two connected emulator boards. The emulator board is being used in the test of the readout board. Preliminary results indicate that the data generated by the emulators can be extracted successfully.

Primary authors: LIU, Chonghan (Southern Methodist University); EDWARDS, Christopher (Fermi National Accelerator Lab. (US)); ZHANG, Li; GONG, Datao (SMU); OLSEN, Jamieson (Fermi National Accelerator Lab. (US)); YE, Jingbo (Southern Methodist University); WU, Jinyuan (Fermi National Accelerator Lab. (US)); LEE, Jongho (Kyungpook National University (KR)); SUN, Quan (Fermi National Accelerator Lab.); LIU, Tiankuan

(Southern Methodist University (US));   LIU, Tiehui Ted (Fermi National Accelerator Lab. (US));   ZHANG, Wei (Southern Methodist University); HUANG, Xing

Presenter: WU, Jinyuan (Fermi National Accelerator Lab. (US))

Session Classification: Programmable Logic, Design Tools and Methods

Track Classification: Programmable Logic, Design Tools and Methods

(Southern Methodist University (US));   LIU, Tiehui Ted (Fermi National Accelerator Lab. (US));   ZHANG, Wei (Southern Methodist University); HUANG, Xing

Presenter: WU, Jinyuan (Fermi National Accelerator Lab. (US))

Session Classification: Programmable Logic, Design Tools and Methods

Track Classification: Programmable Logic, Design Tools and Methods