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System Integration of ATLAS ITK Pixel DCS ASICs

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During the ATLAS phase II upgrade, the tracking system of the ATLAS experiment will be replaced by an all-silicon detector called the ITk (Inner Tracker) with a pixel detector as the most inner part. The control and monitoring data of the new system will be aggregated from an on-detector ASIC called MOPS (Monitoring Of Pixel System) and sent to the DCS using a new interface called MOPS-HUB. The hardware components of the MOPS-HUB, firmware specifications for the FPGA of MOPS-HUB and its integration plan will be presented. In addition, an irradiation plan for the new system will be introduced.

Summary (500 words)

The ATLAS experiment will get a new inner tracker (ITk) during the phase II upgrade. The innermost part will be a pixel detector. After the upgrade, the pixel detector will have 5 times more modules than the present state. The ATLAS pixel detector will use a serial powering scheme to reduce the number of services inside the detector volume, therefore a new DCS (Detector Control System) is being developed at the University of Wuppertal to fulfill the control and monitoring requirements of the new pixel detector. The new DCS has an ondetector ASIC called MOPS (Monitoring Of Pixel System) to monitor the voltages and temperatures of the detector modules and other sub-detector components. A system integration plan of the MOPS chip that includes powering and communication has been proposed with MOPS-HUB as the central unit. MOPS-HUB is an interface between the ITk pixel monitoring ASICs and the DCS. It will aggregate measurement data from the new MOPS chips and send all the values out to the DCS control station. Besides that, the MOPS-HUB FPGA will have a control and monitoring (voltage / current) capability on the connected Controller Area Network (CAN).

The core unit of MOPS-HUB will be the MOPS-HUB FPGA. The Firmware design of the MOPS-HUB FPGA will allow the communication with the MOPS chips over CAN bus using an integrated CAN controller and a physical layer. In addition, the data aggregated between MOPS-HUB FPGA and the DCS will go through different stages. First, MOPS-HUB FPGA will communicate with an Embedded Monitoring and Control Interface (EMCI) through low power differential signals called elinks. Second, the EMCI will serve as a bidirectional channel interface that will transmit the data through a high-speed optical link to an Embedded Monitoring Processor(EMP), which is placed in a non-radiation environment. The EMP will deliver the data to the DCS by means of an Ethernet connection. Some special requirements on the design and firmware is also considered (e.g TMR) since MOPS-HUB will be placed in a radiation environment. The hardware components of the MOPS-HUB, firmware specifications for the FPGA of MOPS-HUB and the integration plans of the new chip will be presented. In addition, an irradiation plan for the new system will be introduced

Primary authors: QAMESH, Ahmed (Bergische Universitaet Wuppertal (DE)); AHMAD, Rizwan (Bergische Universitaet Wuppertal (DE)); KCKER, Dominic (Bergische Universitaet Wuppertal (DE)); Mr FISCHER, Theodor (Technische Hochschule Köln); KARAGOUNIS, Michael (Fachhochschule Dortmund Univ. of Applied Sciences and Arts (DE)); KIND, Peter (Bergische Universitaet Wuppertal (DE)); KERSTEN, Susanne (Bergische Universitaet Wuppertal (DE)); Dr KRAWUTSCHKE, Tobias (Technische Hochschule Köln); Mr SCHREITER, Lucas (Fachhochschule Dortmund, University of Applied Sciences and Arts); ZEITNITZ, Christian (Bergische Universitaet Wuppertal (DE))

Presenter: QAMESH, Ahmed (Bergische Universitaet Wuppertal (DE))

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