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The LHCb Vertex Locator fast calibration

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The LHCb Experiment was upgraded to a trigger-less system reading out the full detector at 40 MHz event rate with all selection algorithms executed in a CPU farm. The upgraded Vertex Locator (VELO) is a hybrid pixel detector read out by the "VeloPix" ASIC with on-chip zero-suppression. This talk describes a novel way of calibrating the VELO detector based on a dedicated firmware, implemented in the control and data acquisition back-end boards of the detector.

Summary (500 words)

The upgrade of the LHCb experiment was installed during the last shut-down of LHC. It transformed the experiment into a trigger-less system reading out the full detector at 40 MHz event rate. The VELO, surrounding the interaction region, is used to reconstruct primary and secondary decay vertices and to measure the flight distance of long-lived particles. It is a hybrid pixel detector read out by the VeloPix ASIC. The highest occupancy ASICs will have pixel hit rates of 900 Mhit/s and will produce an output data rate over 15 Gbit/s, adding up to 1.6 Tbit/s of data for the 40 Mpixels of the whole detector.

Currently, the detector is under commissioning and one of the important tasks to ensure a good performance is a proper calibration of all the front-end channels. The VeloPix readout chip foresees a pixel threshold scan mode based on in-pixel built-in hit counters and a full matrix slow control link access. It was found that the in-pixel counters are affected by the ASIC operation, therefore a new calibration architecture was designed. Instead of counting noisy hits simultaneously in the whole matrix, a few pixels will send hits through fast DAQ links to the back end boards where they will be counted. The back-end firmware is divided in two: one placed in the control boards, and the other one in the DAQ boards. For the former, the control firmware scans over all the front-end pixels for all the chips at the same time. For the latter, the DAQ firmware simultaneously counts 32 pixels per chip. The pixels counted are assigned in a pool architecture, which is common for all the front-end ASICs connected to a single DAQ board. The resources needed to allocate the DAQ firmware in the experiment FPGA (Intel Arria 10) are less than 5% of logic and less than 0.2% of memory.

The full detector calibration time is faster and more deterministic on the firmware calibration than the VeloPix built-in counters mentioned before. The first one is estimated to take a couple of minutes per scan while the second one takes around 15 minutes for a single module and the scaling to the whole detector is not completely linear as it relies on CPU software rather than hardware. Having short calibration times also allow us to have more frequent calibration and more time for physics data taking.

This calibration mode will be used in dedicated data taking runs during the whole VELO Upgrade I operation (2022-2030). The firmware is going to be framed within scans of different characteristics of the front-end like: Threshold, I-V, Charge Collection Efficiency (CCE), etc.

This presentation describes the way this procedure synchronously calibrates all the 624 front-end ASICs, its physical implementation on the LHCb off detector electronics (control board firmware, DAQ board firmware and control and synchronicity of the different cards), as well as the status of the development.

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