TWEPP 2022 Topical Workshop on Electronics for Particle Physics

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The NA62 liquid krypton electromagnetic calorimeter fast readout implementation, commissioning and data taking performance

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The NA62 experiment at the CERN SPS aims to measure the branching ratio of the very rare kaon decay $K^+ \to \pi^+ \nu\bar{\nu}$. The calorimeter level 0 trigger identifies clusters in the electromagnetic and hadronic calorimeters. Along with the trigger data sent to the L0 trigger processor, readout data is collected to be sent to L1 software trigger level. In this work we present the novel implementation of the readout data collection and forwarding system in the multiple layers of the calorimetric trigger structure. We will also present the commissioning of the system and the performance evaluation on current data taking.

Summary (500 words)

The NA62 experiment aims to measure the very rare kaon decay $K^+ \to \pi^+ \nu\bar{\nu}$, collecting O(100) events with a 10% background to make a stringent test of the Standard Model and deepen the knowledge of the CKM matrix. The $K^+ \to \pi^+ \nu\bar{\nu}$ decay is highly suppressed, well known from the theoretical standpoint and very sensitive to many New Physics models. The Standard Model branching ratio prediction for $K^+ \to \pi^+ \nu\bar{\nu}$ is $(8.4 \pm 1.0) \times 10^{-11}$.

The calorimeter level 0 trigger is used to suppress one of the main backgrounds, the $K^+ \to \pi^+ \pi^0$ decay, and to select events with a π^+ in the final state. It identifies clusters in the electromagnetic and hadronic calorimeters and prepares time-ordered lists of the reconstructed clusters together with the arrival timestamp, position, and energy measurements of each cluster. It also provides trigger decisions based on complex combinations of energy and cluster multiplicity. The main features of the trigger processor are the high design hit rate (30 MHz) and the required single cluster time resolution (1.5 ns). The calorimeter trigger processor is a parallel system composed of 37 boards, 111 mezzanines and 221 programmable devices housed in three 9U crates.

Until now, only trigger data was available to L0 trigger processor, while readout data was not sent to L1 software trigger layer. The implementation of the novel readout datapath towards L1 has now been deployed, in order to make readout data available to the TDAQ layer and to enhance data acquisition efficiency and refine trigger decision between hardware L0 and software L1 trigger layers.

At the early stage in the first hardware layer, the trigger signal arriving from L0 Trigger processor is used to collect timestamps of the triggered data, calculated with proper delay offset. Energy peak data calculated from CREAM modules are stored in proper buffers (separated from trigger data line), and data timestamps are matched with trigger timestamps within a programmable window. Selected data is then forwarded to higher levels in the tree structure of the system, using the same data path as the trigger data lines with proper traffic priority rules; this expedient allows to use completely the same hardware already deployed, except from a mezzanine card at the second hardware layer (also called merger layer), implementing a custom made dual Gigabit ethernet interface that has been added later. Data packets are then formed with event and peak information using the standard NA62 multi-event packet (MEP) format, and thus are sent to the data acquisition computing farm in order to enhance data selection. A total of 7 mergers are present, sending data in parallel.

The new fast readout system has been put on-line in the experiment with the beginning of 2022 data taking run, after a commissioning phase. Performance measurement has been carried out with synthetically gener-

ated data at the beginning of the readout datapath, in order to check readout and trigger data integrity with increasing beam intensity.

Primary authors: AMMENDOLA, Roberto (INFN e Universita Roma Tor Vergata (IT)); SALAMON, Andrea (INFN e Universita Roma Tor Vergata (IT))

Co-authors: ALIBERTI, Riccardo (Johannes Gutenberg Universitaet Mainz (DE)); BARBANERA, Mattia (Universita e INFN, Perugia (IT)); BIZZARRI, Marco (Universita e INFN (IT)); BONAIUTO, Vincenzo (INFN e Universita Roma Tor Vergata (IT)); BORETTO, Marco (CERN); CECCUCCI, Augusto (CERN); CHECCUCCI, Bruno (Universita e INFN, Perugia (IT)); DE SIMONE, Nico (CERN); FANTECHI, Riccardo (Universita & INFN Pisa (IT)); FEDERICI, Luca (Universite Catholique de Louvain (UCL) (BE)); LUPI, Matteo (CERN); LURKIN, Nicolas (Universite Catholique de Louvain (UCL) (BE)); MASSRI, Karim (CERN); MIRRA, Marco (Universita e sezione INFN di Napoli (IT)); PARKINSON, Christopher John (University of Birmingham); PEDRESCHI, Elena (Universita & INFN Pisa (IT)); PIANDANI, Roberto (University of Chinese Academy of Sciences (CN)); PICCINI, Mauro (INFN - Sezione di Perugia (IT)); RUGGIERO, Giuseppe (Lancaster University (GB)); RYJOV, Vladimir (CERN); SALINA, Gaetano (Istituto Nazionale di Fisica Nucleare); SARGENI, Fausto (INFN e Universita Roma Tor Vergata (IT)); SERGI, Antonino (INFN e Universita Genova (IT)); SOLDI, Dario (Universita e INFN Torino (IT)); SPINELLA, Franco (Universita & INFN Pisa (IT)); VENDITTI, Stefano (CERN); ZAMKOVSKY, Michal (Universite Catholique de Louvain (UCL) (BE))

Presenter: AMMENDOLA, Roberto (INFN e Universita Roma Tor Vergata (IT))

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