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DTS-100G - A versatile heterogeneous FPGA board for cryogenic sensor readout

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Heterogeneous SoC-FPGAs are extremely valuable in custom instrumentation. We present the joint development of the DTS-100G by DESY and KIT. It is built around a Xilinx Zynq Ultrascale Plus and offers all available high-speed transceivers using QSFP28, Firefly28G, FMC, and FMC+ interfaces. The board is not specialized to a single application and can be used as a generic DAQ platform for various physics experiments. DTS-100G was successfully developed, built, and commissioned. ECHo-100k is the first experiment, which will employ the board. This contribution will show the system architecture and explain how DTS-100G is a crucial component in the DAQ chain.

Summary (500 words)

Heterogeneous FPGAs, the combination of various processors with programmable logic in a single chip, are extremely valuable in custom instrumentation. This is because they allow tight integration of additional functionality directly on the chip, including slow control, configuration, and calibration, thereby profiting from the tight coupling of processor and programmable logic. In this contribution, we present our custom heterogeneous FPGA board DTS-100G. It is built around a Xilinx Zynq Ultrascale Plus (ZUS+) 11EG (or footprint compatible devices) and utilizes all high-speed transceivers. The full support of all transceivers is barely the case for currently available commercial system-on-modules (SoM).

The board is not tailored to a specific experiment but will be used as a generic DAQ platform for many smaller physics experiments. Furthermore, it was designed to evaluate different optical 100G technologies. The processing system of the ZUS+ is connected to a SoDIMM slot (16 GB DDR4 maximum), an M.2 slot (SATA or PCIe link), a DisplayPort, USB3.0, 1Gb/s Ethernet, 2 UART over USB (FTDI), 2x1 Gb QSPI Flash, MicroSD 3.0, and an EEPROM. The programmable logic is connected to one FMC+, two FMC connectors, a QSFP28 connector, and a four-lane FireFly28G connector. Furthermore, 4 GB of DDR4 PL RAM and GPIO are attached to the PL. The FMC+ connector integrates 8 GTY (max. 28 Gb/s per link), 16 GTH (max. 16 Gb/s per link), 77 HP and 3 HD LVDS links. The FMC interfaces are primarily used to attach NVME storage to the PL for performance evaluation. One FMC connector has 8 GTH, 17 HP, and 17 HD links. The second FMC connector has 8 GTH and 20 HP links. Version 1 of DTS-100G was successfully developed, built, and commissioned. Currently, the link performance evaluation is ongoing for different scenarios.

The first experiment, which will use the board, is the Electron Capture in Holmium (ECHo-100k) experiment. ECHo measures the electron capture process of Holmium-163 decay. The isotope is directly embedded in the absorber of the superconducting sensor. Large arrays of metallic magnetic calorimeters in a cryostat at 20 mK are used for the measurement. The parallel readout is performed utilizing microwave squid multiplexing. Demultiplexing at room temperature requires parallel processing of 4 GHz of analog bandwidth ranging from 4-8 GHz. Therefore, the DAQ uses an analog IQ mixing stage, a conversion board with 10 ADC-Channels (1GSPS each), and 12 DAC-Channels (2.8GSPS each) attached to our DTS-100G board at the FMC+ connector. ADC and DAC feature a JESD204B interface connected with high-speed differential pairs to the GTH and GTY transceivers and HP links for configuration. The FPGA implements the complete digital signal processing chain for demultiplexing and event detection. Detected events are packed and forwarded to the PS, linked to the server backend. This approach is possible because of the substantial data reduction in the processing chain. It is noteworthy that no commercial FPGA board satisfied the requirements of the ECHo DAQ. This

contribution will show the system architecture and explain how DTS-100G is a crucial component in the DAQ chain.

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