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Data-Driven Design of the Belle II Track Segment Finder

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The Belle II experiment relies on a level-1 trigger system to reduce background and preselect events of interest for particle physics. The Central Drift Chamber is the main track detector which makes its trigger system important for online track reconstruction. To improve its hit efficiency a new extension of the track segment finder for low angel tracks is designed. By combining hardware and software development flows, an automated data-driven pipeline is created and three different-sized hardware concepts are implemented. The operation point is adjustable to balance hit efficiency against hit purity in the trigger system.

Summary (500 words)

In this work, a new track segment finder (TSF) is developed as part of the level-1 trigger system of the Belle II Central Drift Chamber (CDC). The developed system enables the detection of particle tracks featuring low angles.

The need for an extension of the current system derives from simulations involving displaced-vertex tracks. It is expected that such events lead to the emittance of electrons, positrons, and muons from outside the interaction point. Because the current TSF is not capable of fully detecting displaced particle tracks, the functionality of the level-1 trigger system is limited. To improve the hit efficiency an extension of the state-of-the-art TSF is introduced. The current system uses an a priori calculated formula to classify occurring patterns for successive trigger decisions. Since this algorithm requires a fixed origin of particle tracks, it is not applicable for the events under investigation.

Therefore, a novel approach is proposed for developing the displaced-vertices TSF utilizing a dataset of simulated decays. Adhering to the latency constraints of the trigger system, a lookup table-based TSF is designed which deposits its classification decision in memory. The proposed concept allows an arbitrary combination of positively hypothesized patterns contributing to a trigger decision. As a result, the algorithmic performance of the module is strongly dependent on the selection of suitable patterns. Therefore, the classifier configuration is identified as a key factor during the development process. An adapted hardware/software co-design methodology allows for concurrent algorithmic optimization and efficient implementation.

Three different-sized hardware concepts of displaced-vertices TSFs are implemented as a proof-of-concept in this work. Their feasibility is proven on the Universal Trigger Board 4 utilizing an FPGAs currently deployed in the Belle II experiment. In addition, algorithmic hardware models are derived for every module. In conjunction with the provided displaced-vertex dataset, an automatic design space exploration is implemented. It is subsequently used to select a suitable classifier configuration based on hyper-parameters. By combining hardware and software development flows, an automated data-driven pipeline is created for the TSF under development. Taking a dataset and hyper-parameters as an input, a fully tested hardware firmware is automatically synthesized and implemented. Furthermore, its algorithmic performance is estimated on a validation set containing simulated dark-matter decays.

To conclude, three hardware concepts for the displaced-vertex TSF are successfully implemented on the Universal Trigger Board 4 and ready for deployment in the level-1 Belle II trigger system. In the future, training of TSF classifiers can be performed automatically. An operation point can be chosen to achieve optimal data pre-processing for successive trigger algorithms by balancing hit efficiency against hit purity. An exemplary

increase of the recall score from 22.4 % to 85.0 % is achieved while reducing the precision score from 94.7 % to 88.2 %.

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