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Commissioning of the new ATLAS Muon Central Trigger Processor Interface (MUCTPI)

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The new Muon-Central-Trigger-Processor-Interface (MUCTPI) is part of the upgrade of the ATLAS Level-1 trigger system for the upcoming run of the Large Hadron Collider at CERN. High-end FPGAs receive and process muon candidate information arriving on 208 high-speed optical serial links, while the board is controlled by a SoC. Processed trigger information and summary data are sent to other parts of the trigger and data acquisition system. This paper describes the hardware setup, the online software as well as the integration and commissioning procedures carried out during the start of LHC Run 3.

Summary (500 words)

1. The ATLAS Trigger System: The ATLAS trigger system (Fig.1), consists of a first-level trigger based on custom electronics and firmware, and a high-level software trigger based on COTS hardware. The first level trigger uses information from calorimeters and muon detectors. The muon trigger detectors in the barrel area are Resistive Plate Chambers (RPC) while the endcap consists of MicroMesh Gaseous Structure (Micromegas) and Thin-Gap Chambers (TGC). The Muon-to-Central-Trigger-Processor-Interface (MUCTPI) receives muon candidate information from all muon sectors and calculates multiplicities. Potential double counting of single muons due to geometrical overlap of the chambers is avoided thanks to overlap handling logic in the MUCTPI. Muon trigger object information is sent to the Topological Trigger Processor (L1Topo), which combines it with trigger objects from the calorimeters for event triggering based on multiple topological criteria. Multiplicities are sent to the Central Trigger Processor (CTP), which combines it with the trigger information from forward detectors, calorimeters and L1Topo and issues the Level-1 accept decision.

2) MUCTPI upgrade:

The new MUCTPI (Fig.2) receives more trigger candidates with more detailed data using optical links instead of electrical ones. It improves the overlap handling by taking into account overlap between octants which was previously impossible. The new MUCTPI is built as a single ATCA blade using two Muon Sector Processor (MSP) FPGAs (Xilinx Virtex Ultrascale), which receive trigger muon information from 208 muon sectors and implement the overlap handling and send trigger objects to L1Topo through optical links. The Trigger and Readout Processor (TRP) FPGA (Xilinx Kintex Ultrascale), combines the trigger information and sends multiplicities to the CTP and trigger data to the DAQ. A System-on-Chip (SoC, Xilinx ZynqMP Ultrascale+) is used for control, configuration, and monitoring of the hardware. The SoC includes programmable logic which allows access to memories implemented in the processing FPGAs. The Processor System (PS) runs an operating system (Centos Linux). In addition, it configures and controls the hardware of the MUCTPI using standard interfaces like I2C. A Gigabit Ethernet connection allows communication with the ATLAS run control system.

3) Online software & commissioning:

The new MUCTPI was installed in the ATLAS counting room (USA15) in 2021 (Fig 3). Physical connections to the interfacing systems were carried out. Namely, the input fibers from the Muon Sector Logic boards, the output fibers to the L1Topo and CTP, as well as other infrastructure items were connected and tested. During dedicated ATLAS testing periods additional integration tests were done together with the interfacing systems to validate communication and data flow. These tests and relevant results will be presented.

4) Conclusions & outlook:

The new MUCTPI was installed in the experiment, and is currently being commissioned to be ready for the start of Run 3 of the LHC. The upgrade motivation will be briefly described, followed by an outline of the integration tests and relevant results, as well as ongoing work, which includes a complete suite of monitoring software that was developed to facilitate the commissioning and operation of the MUCTPI.

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