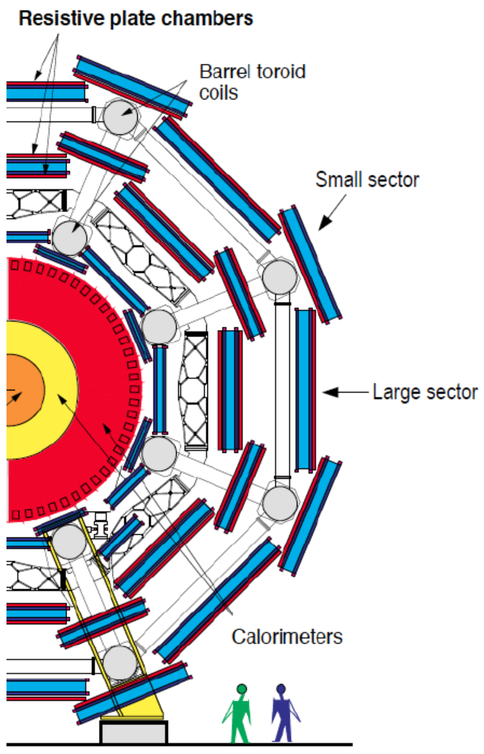
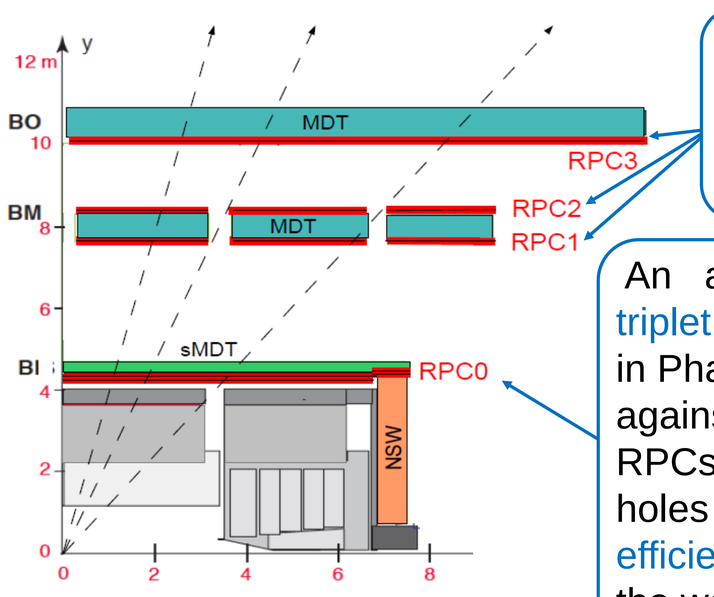
STATUS OF THE LEVEL-0 ATLAS BARREL MUON TRIGGER FOR HIGH-LUMINOSITY LHC

Topical Workshop on Electronics for Particle Physics (TWEPP)
19-23 September 2022, Bergen, Norway



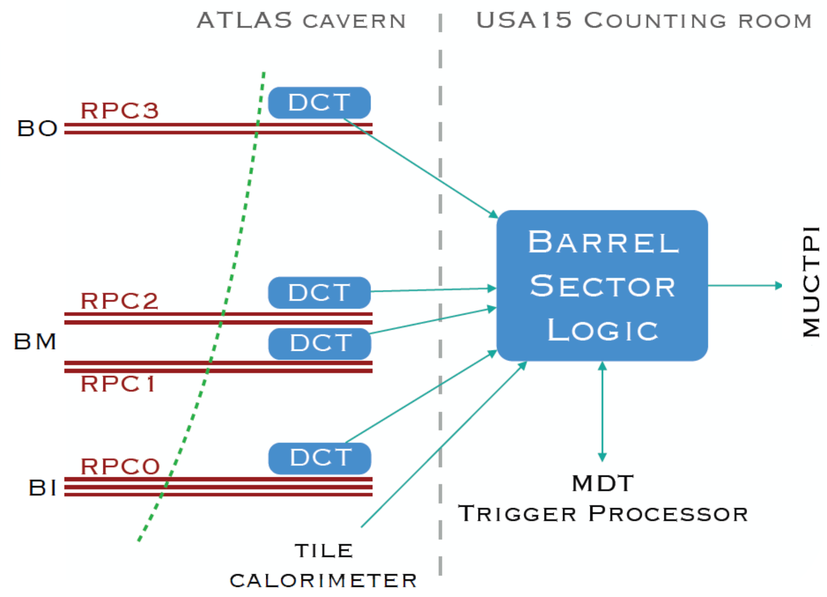
Phase-II RPC-based L0 Trigger

Phase-II upgrade in LS3 (2026-2028): preparation for High-Luminosity LHC and Run 4



3 Resistive Plate Chamber (RPC) doublet layers (**BM/BO**) in Run 1-3 will be kept also at HL-LHC.

An additional inner layer of triplet RPCs (**BI**) will be added in Phase-II upgrade to be robust against inefficiencies of legacy RPCs and to cover acceptance holes (reaching 92% of efficiency times acceptance in the worst case scenario) [1].



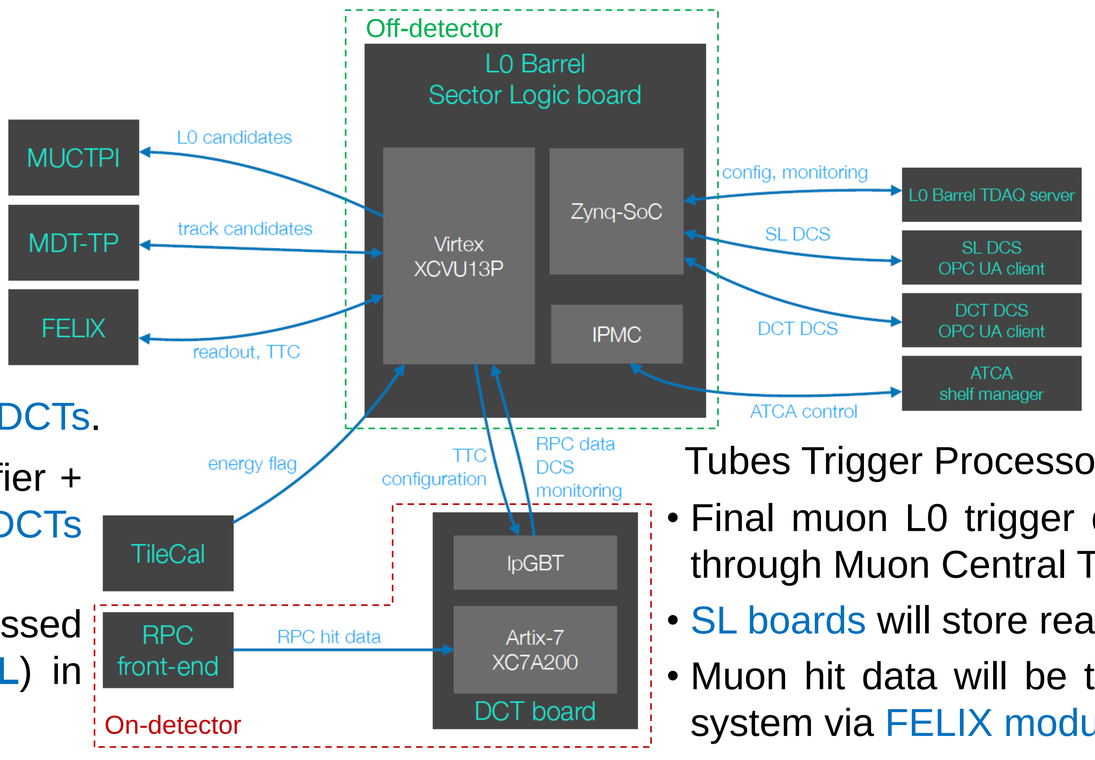
RPC-based trigger requirements: up to 100 kHz trigger rate and 390 ns latency.
Global L0 trigger requirements: up to 1 MHz trigger rate and 10 μs latency [2].

RPC L0 Trigger: hit coincidence in at least 3 chambers out of 4 or coincidence in BI and BO layers.

Trigger and Readout

On-detector

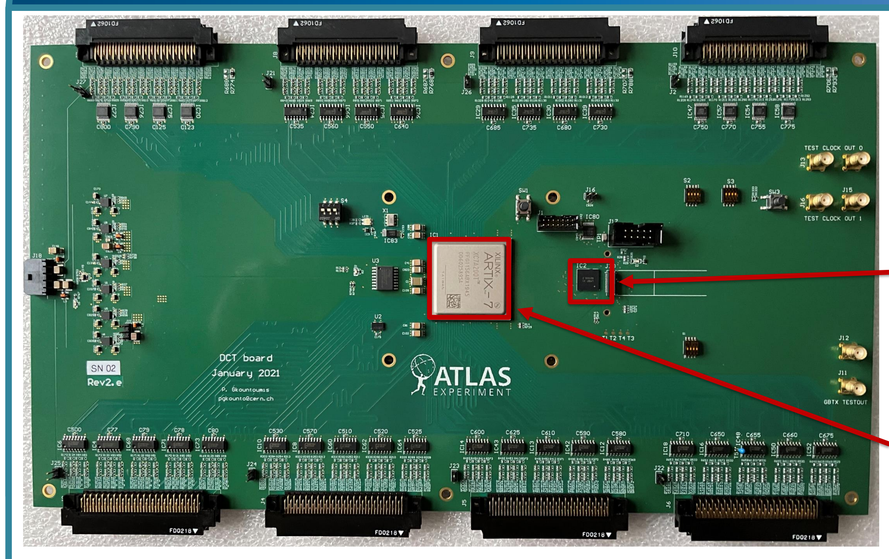
- Current trigger and readout electronics (except for front-end boards) will be replaced by 1570 Data Collector and Transmitter (**DCT**) boards.
- Front-end boards will collect RPC hit data and send them to DCTs.
- BM/BO DCTs will include amplifier + discriminator, while BI DCTs amplifier + discriminator + TDC.
- DCTs will send zero suppressed data to barrel Sector Logic (**SL**) in counting room (USA15).



Off-detector

- 32 barrel SL boards will receive all the RPC data and control the DCTs.
- Each SL board will be connected with up to 50 DCTs through optical fibres.
- SL boards will produce trigger candidates based on RPC and Tile Calorimeter data and will interface with the Monitored Drift Tubes Trigger Processor (**MDT-TP**) for further refinements.
- Final muon L0 trigger decision will be sent to ATLAS central trigger through Muon Central Trigger Processor Interface (**MUCTPI**) board.
- SL boards will store readout data into local memories.
- Muon hit data will be transmitted to High Level Trigger and readout system via FELIX modules when an L0-Accept signal will be received.

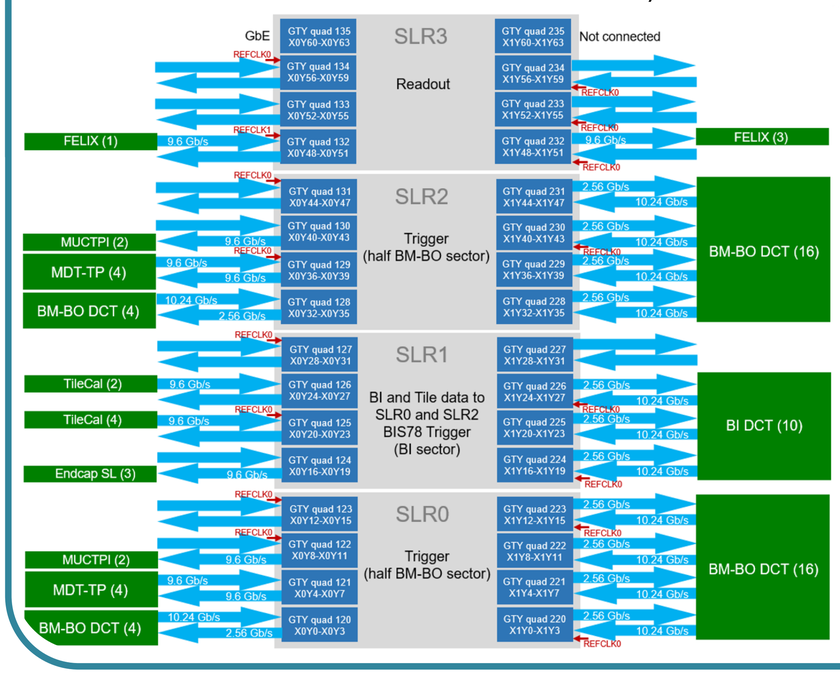
DCT board

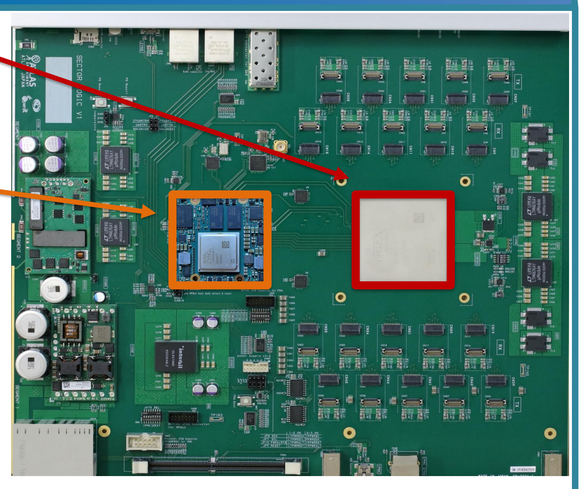


- The **DCT** is based on a Xilinx Artix-7 **FPGA**.
- FPGA performs 1.2 Gb/s TDC (only for BM/BO) and zero suppression.
- **DCT** connects to SL via bidirectional optical fibres.
- The Low Power Gigabit Transceiver (**lpGBT**) ASIC handles the DCT-SL serial data transmission.
- FPGA firmware ready and simulated with MC data.
- BM/BO DCT prototype tested with an RPC detector.
- Radiation qualification to be completed in 2023.

SL board

- The **SL** board is based on a Xilinx Virtex Ultrascale+ **FPGA** (XCVU13P).
- A **SoC** module (Xilinx Zynq Ultrascale+) interfaces with the DCSs and TDAQ server.
- IPCM module will send monitoring data to the ATCA shelf-manager.
- SL FPGA will receive all RPC data, reorder them by Bunch Crossing number, perform L0 trigger algorithm and readout.





- SL FPGA is divided into 4 Super Logic Regions (SLRs).
- Firmware logic and I/O ports are placed as in the scheme on the left.
- Firmware ready and simulated.
- SL board prototype ready, functionalities tested in lab.
- Test with DCT prototype and other interfaces to be completed in 2023.

[1] ATLAS Collaboration. *Technical Design Report for the Phase-II Upgrade of the ATLAS Muon Spectrometer*. CERN-LHCC-2017-017.
[2] ATLAS Collaboration. *Technical Design Report for the Phase-II Upgrade of the ATLAS TDAQ System*. CERN-LHCC-2017-020.

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