Silent and slim DC-DC converters for the CMS MTD BTL and ECAL Barrel for HL-LHC.

TWEPP 2022

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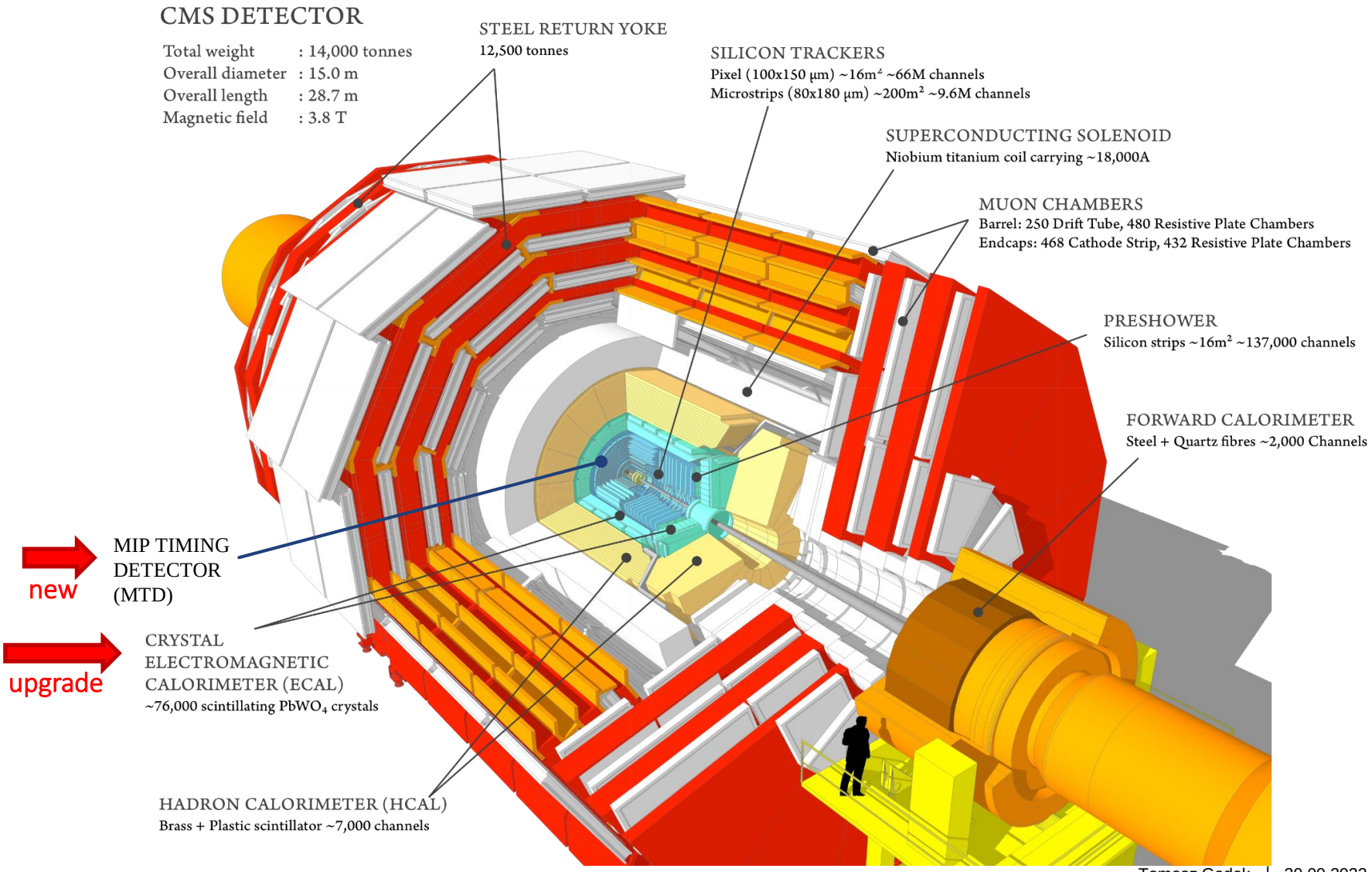
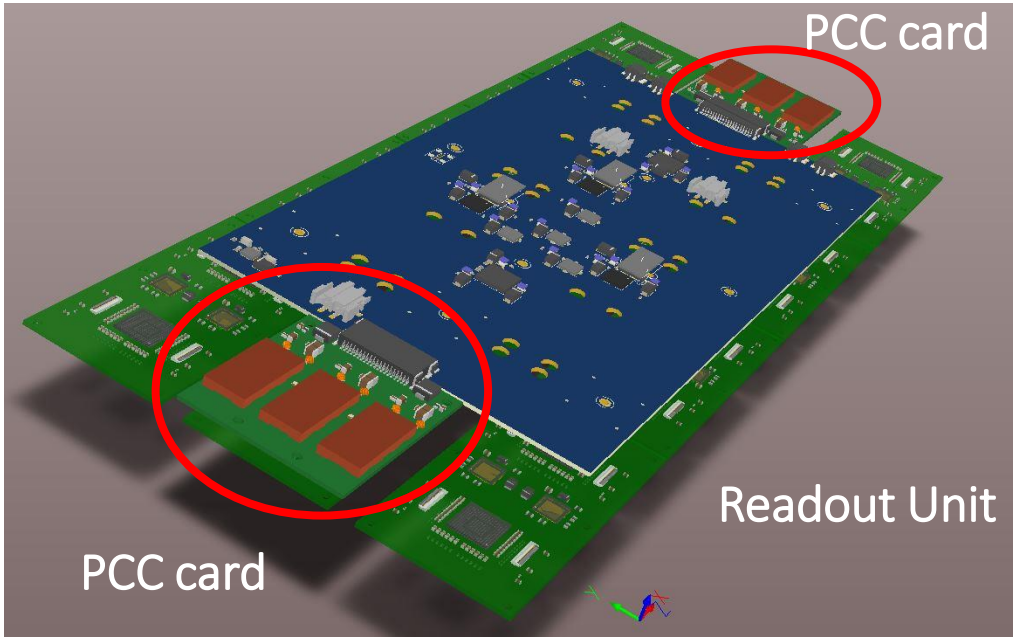
on behalf of the CMS collaboration

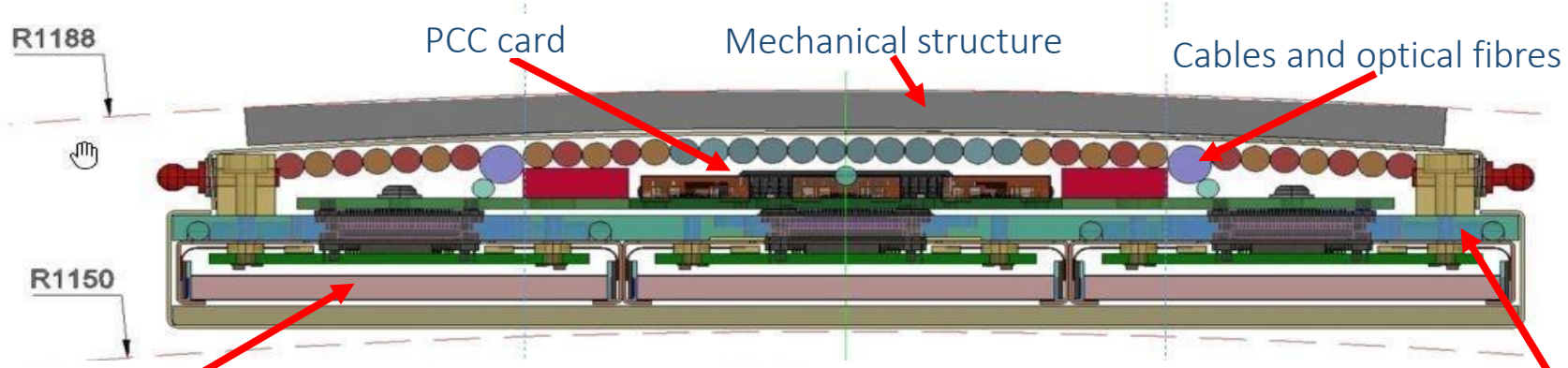
Introduction - LS3 of LHC



DC-DC converters in CMS MTD BTL

- **Barrel Timing Layer:**
  - **432 Readout Units, each powered by 2 Power Conversion Cards (PCCs).**
  - **Single PCC hosts 3 DC-DC converters.**
  - **Production volume assumes nearly 1000 PCCs, carrying 3000 DC-DC converters.**

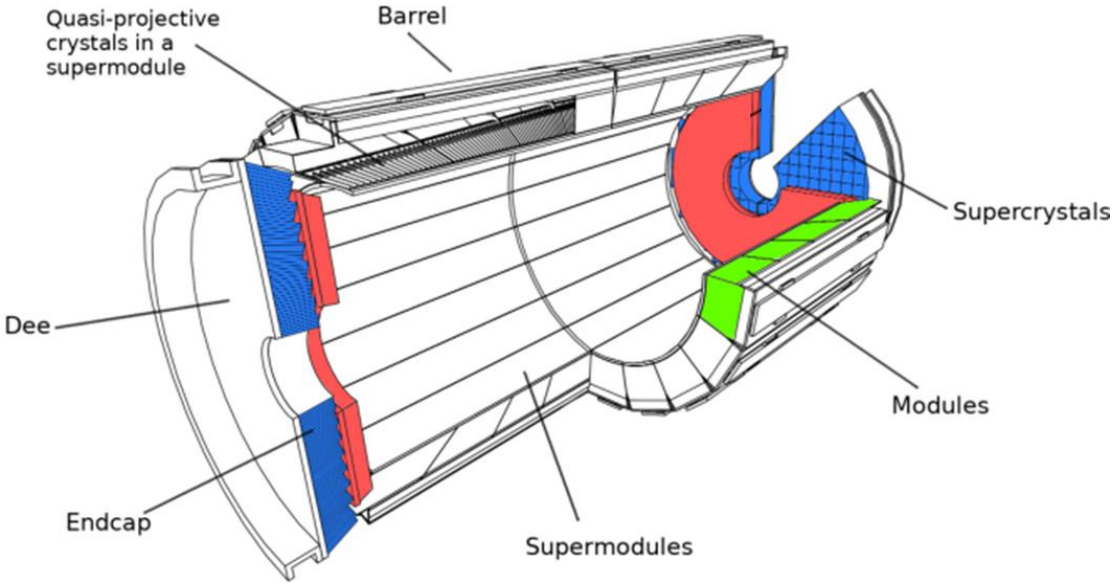




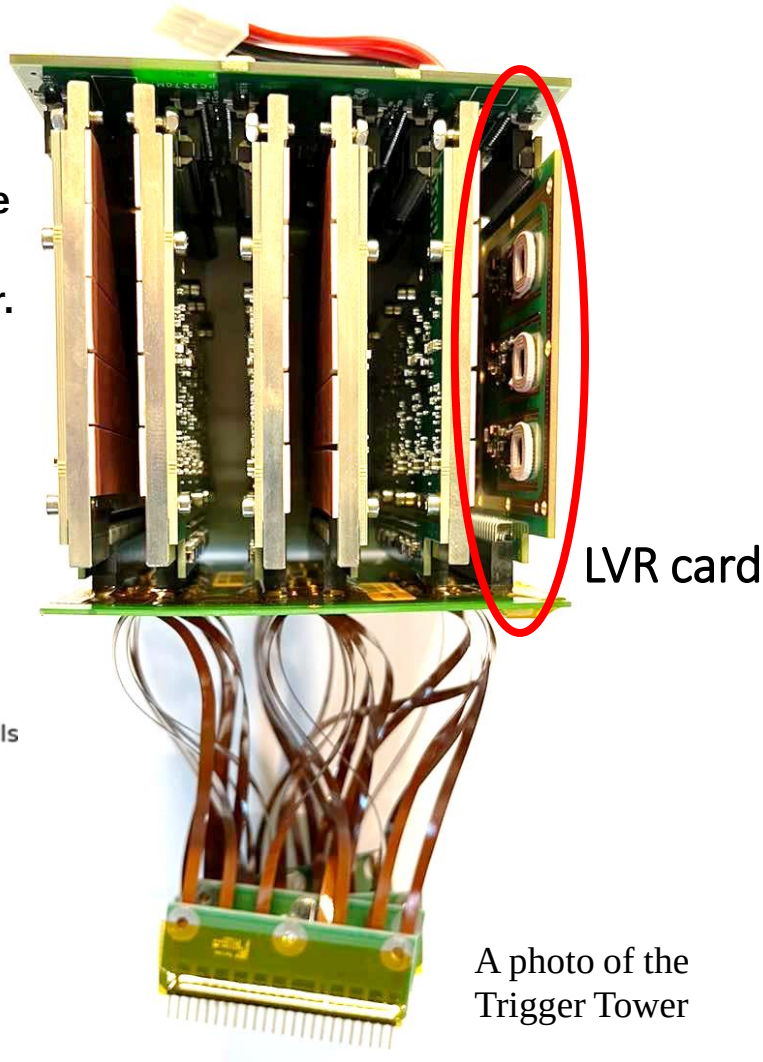
Radial view of the Readout Unit placement in the sub-detector

DC-DC converters in CMS ECAL Barrel

- **Electromagnetic Calorimeter Barrel:**
  - **Upgrade of an existing sub-detector.**
  - **Mechanics and PCB outlines as in legacy system.**
  - **2448 Trigger Towers, each powered by 1 Low Voltage Regulator Card (LVR).**
  - **LVRs host 4 DC-DC converters and 1 linear regulator.**
  - **Production volume will reach nearly 3000 LVRs, carrying 12,000 DC-DC converters.**



A structural sketch of the CMS ECAL



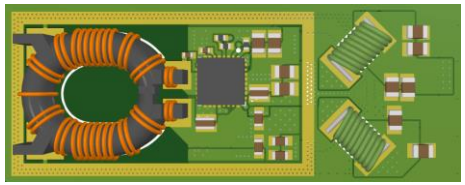
A photo of the Trigger Tower

On detector DC-DC conversion environment

Single converter operating requirements	
Integrated dose	32 kGy [BTL]
Luminosity	1.90×10^{14} n_{eq}/cm^2 [BTL]
Magnetic field	3.8 T [both]
Max. Length	45.0 mm [ECAL]
Max. Width	18.0 mm [ECAL]
Max. Height with PCB	7.0 mm [BTL]
Min. temperature	-35ºC [BTL]
Max. temperature	+30ºC [ECAL]
Input voltage	8-12 V DC [both]
Output voltages	1.2, 1.8, 2.5 V [BTL]
Max. load	3.4 A at 1.8 V [BTL]

Common DC-DC converter design block to fit both experiments.

FEAST2?



bPOL12?

History of prototype cards development

Photo of PCC v02 with the test adapter

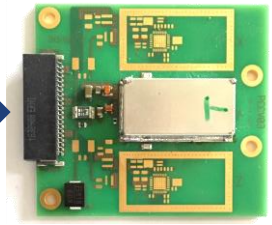


Photo of PCC v03

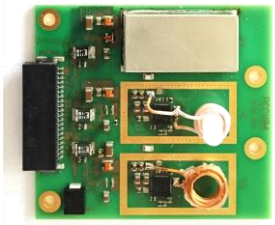
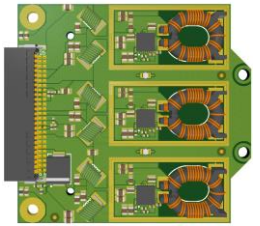


Photo of PCC v04

Photo of PCCi v1



Picture of the 3D model of PCCi v3

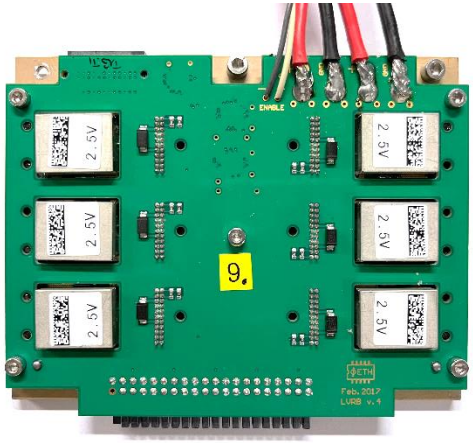


Photo of LVR v1

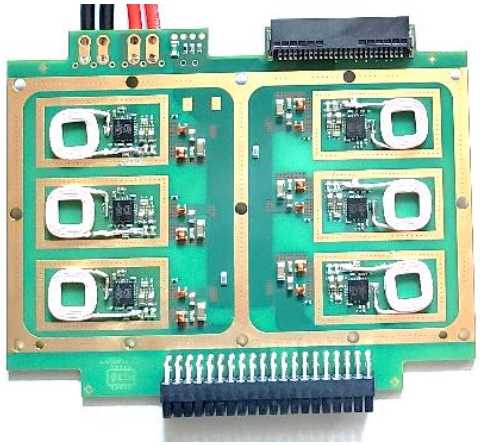


Photo of LVRi v2

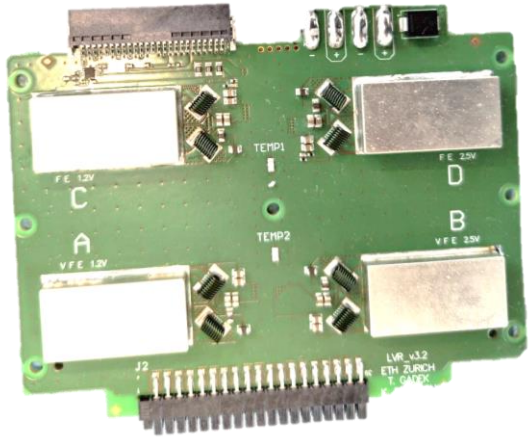
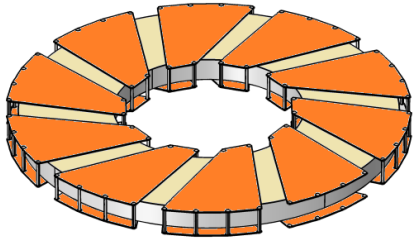


Photo of LVRi v3

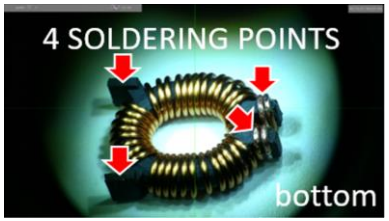
Main inductor choices



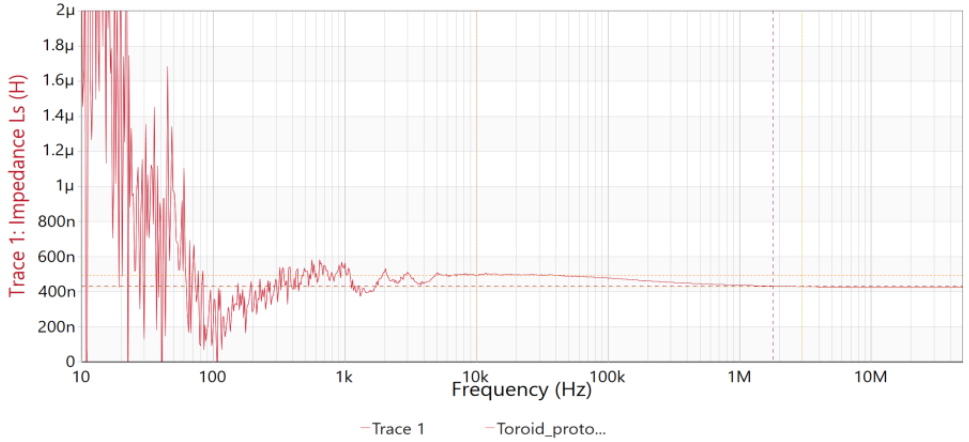
Toroidal PCB integrated inductor	Litz copper wire solenoid	Solid copper wire toroid
+ cheapest - integrated in PCB **+ slimmest possible design**	**+ medium price ~2 CHF/pc** **+ 1.6 mm thick** **+ lowest DCR (21 mΩ)**	**+ price similar to Litz solenoid** **+ low DCR (26 mΩ)** **+ low emission in near fields** **+ lowest inductance loss when shielded**
- L > 150 nH requires big PCB area (>13x13 mm^2) and/or thicker PCBs (3-5 mm) - High DCR in 35 to 70 um copper 1.6 mm stack-ups - Big losses/lowest efficiency	- 30-40% inductance loss when shielded - Efficiency loss when shielded - Biggest H near field emission - Requires encapsulation to prevent movement/vibration in magnetic field	- 4.5 mm thick - Requires tallest shield

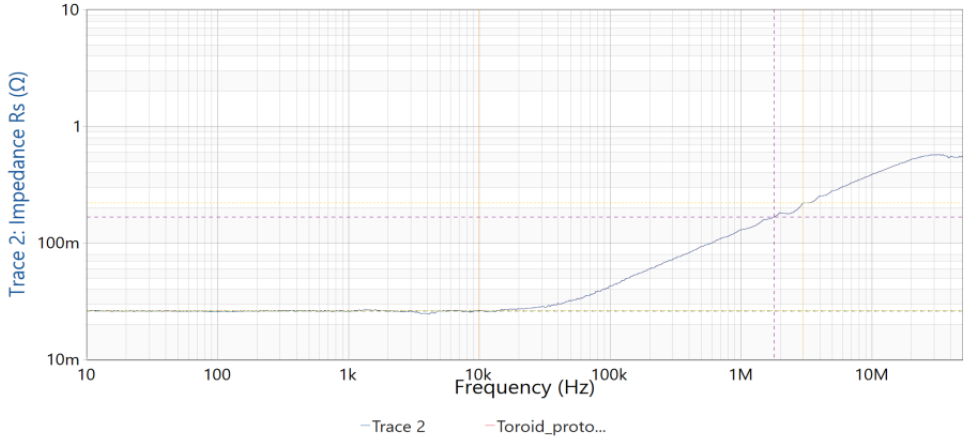
Main inductor - toroid

- **Prototype toroid properties:**
- ~490 nH measured at 10 kHz,
- ~430 nH measured at 1.8 MHz
- ~26 mΩ DC resistance
- 4 soldering points – firm fixation to a PCB
- Outer dimensions: 17.4 x 14.2 x 4.5 [mm]^3
- 2 companies contacted for production of 650 pieces, 1 production lot received



Photos of hand-made prototype toroid (top, bottom and side views)

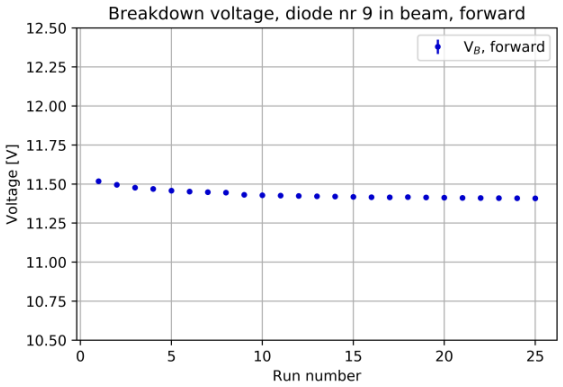




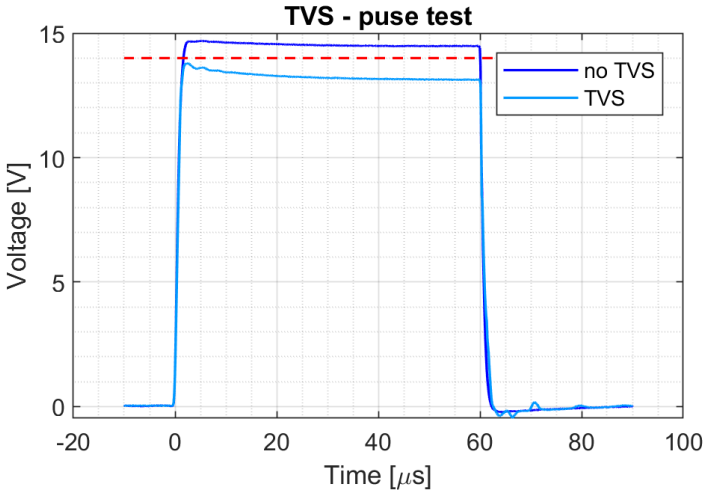
	Cursor 1	Cursor 2	Cursor 3
Frequency	10 Hz	10 kHz	1.8 MHz
Trace 1	**Ls**	**Ls**	**Ls**
Measurement	2.331 µH	491.824 nH	431.166 nH
Trace 2	**Rs**	**Rs**	**Rs**
Measurement	26.104 mΩ	26.412 mΩ	167.232 mΩ

Overvoltage protection

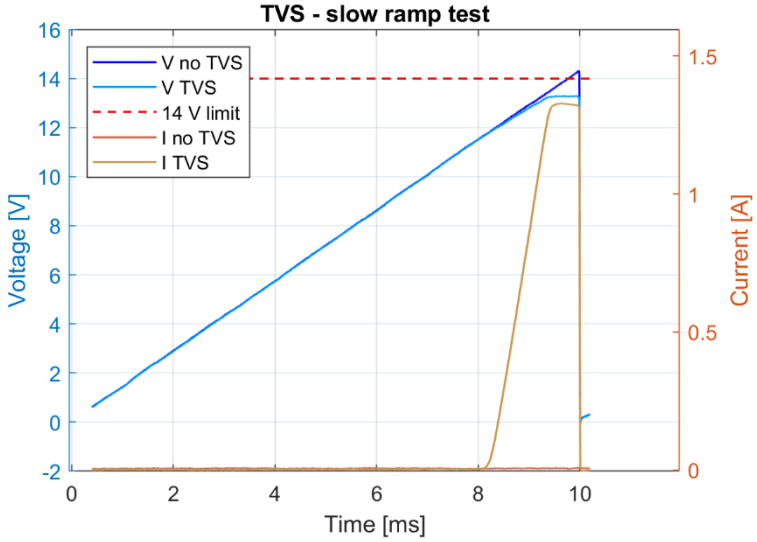
- **Overvoltage protection:**
  - FEAST and bPOL converters are vulnerable to overvoltages > 14 V.
  - Properties of TVS (transient votage suppression) diode are being evaluated.
- **Littlefuse SMCJ10CA:**
  - Radiation test showed good stability of the breakdown voltage.
  - Test with 1 A pulse amplifier gave promising results.



Breakdown voltage stability of SMCJ10CA up to 1.5 x 10^{14} protons *(80 kGy). Credits: Pascal Larent Bebie.*



Waveform: 60 µs pulse above 14 V.

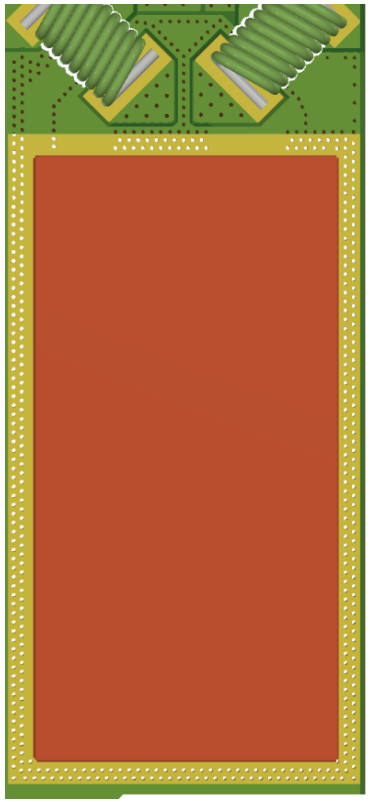


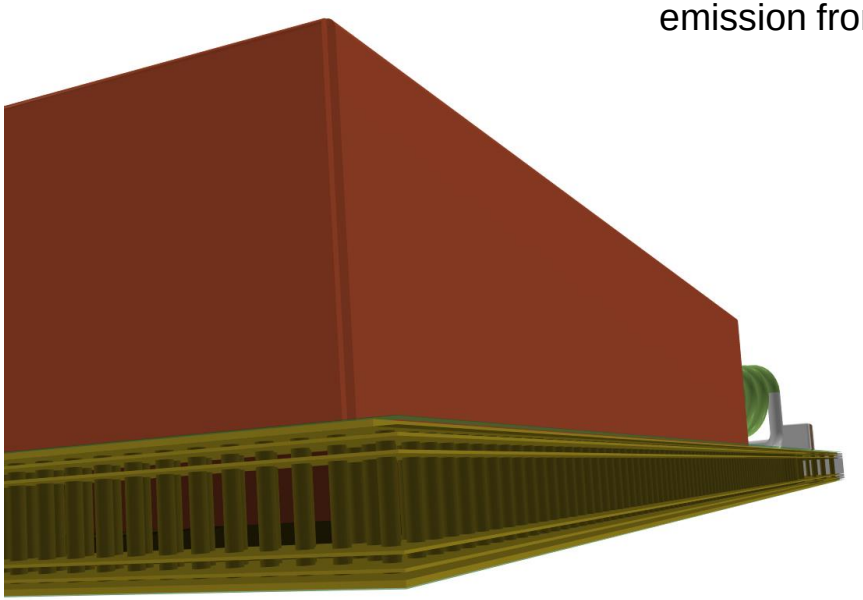
Waveform: Slow ramp test. Blue – voltages, orange – currents.

Shielding – near field

- **Shield choice:**
  - **300 um copper tin coated, 30x15x5 mm^3 with the following layout features:**

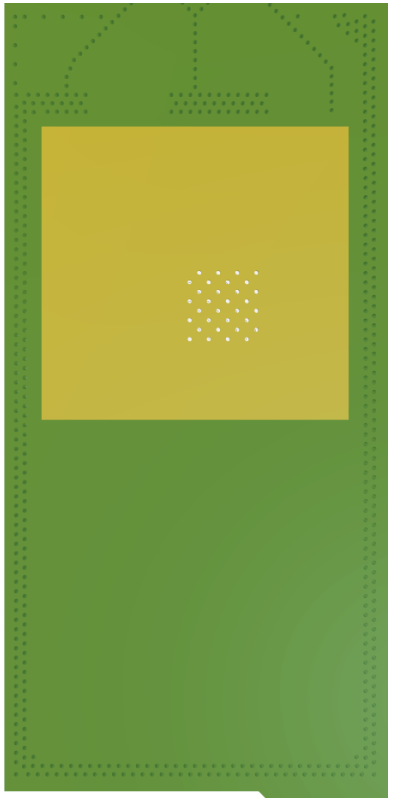
Shield soldered all around.





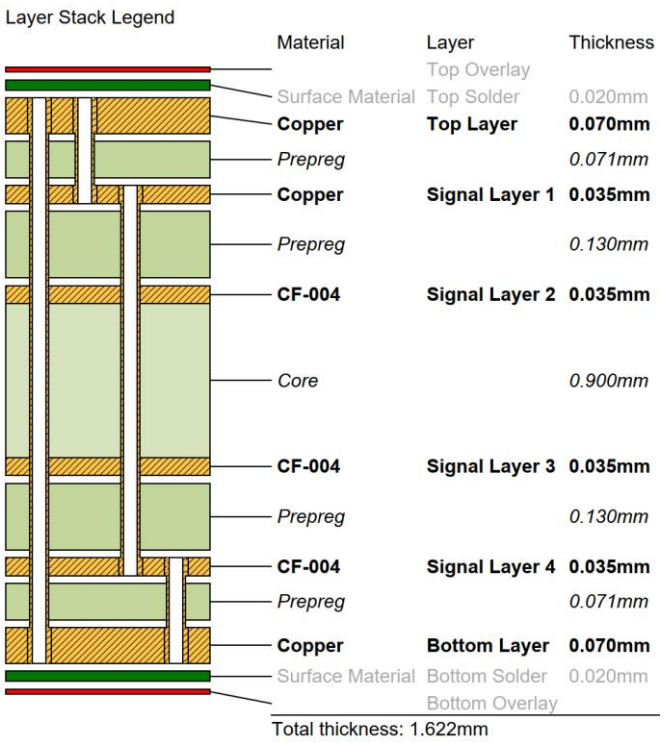
Dual guard ring of vias to weaken emission from the PCB sides.

3 complete layers of copper to attenuate emission from the bottom of the PCB.

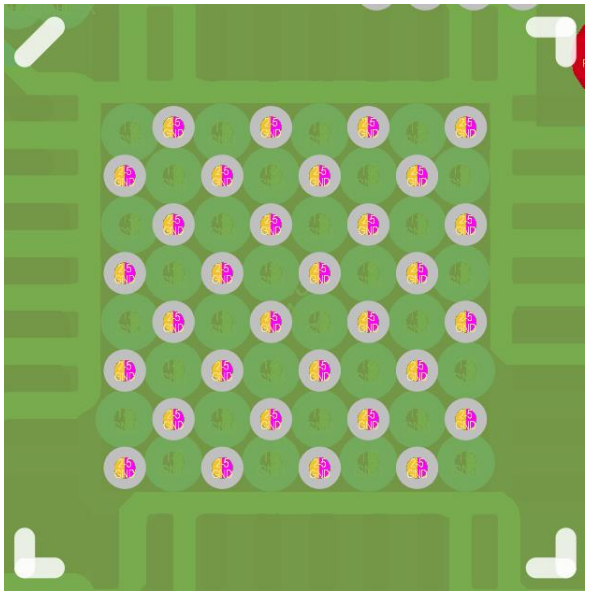


Shielding – near field

- **Routing under the shield:**
  - **Use of blind and buried vias to switch layers of the signals - no through holes in the shielded region.**
  - **Thermal interface under the ASIC using staggered vias for the layers 1-2, 2-5, 5-6.**

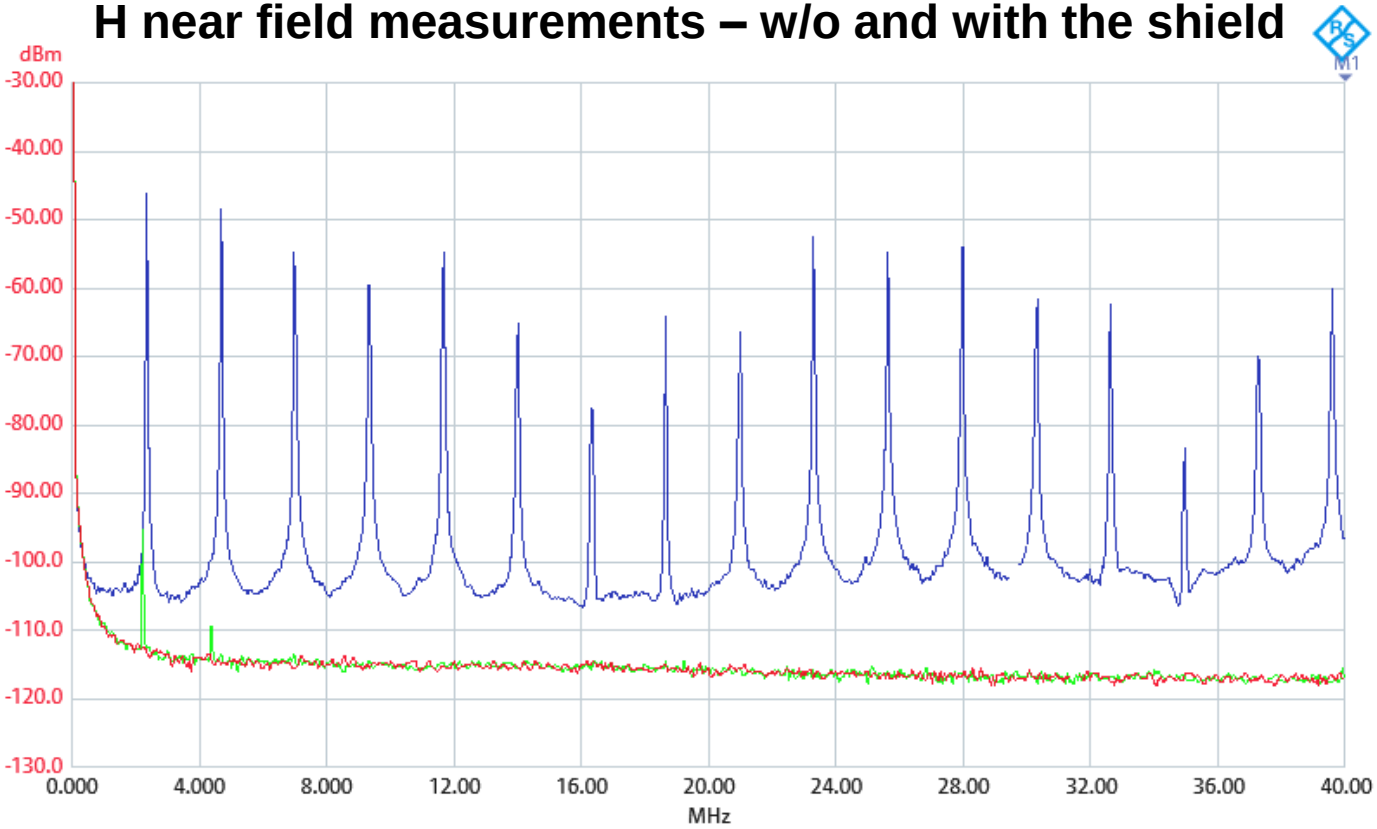


Staggered vias, creating a large heatsink under the ASIC.



Shielding effectiveness

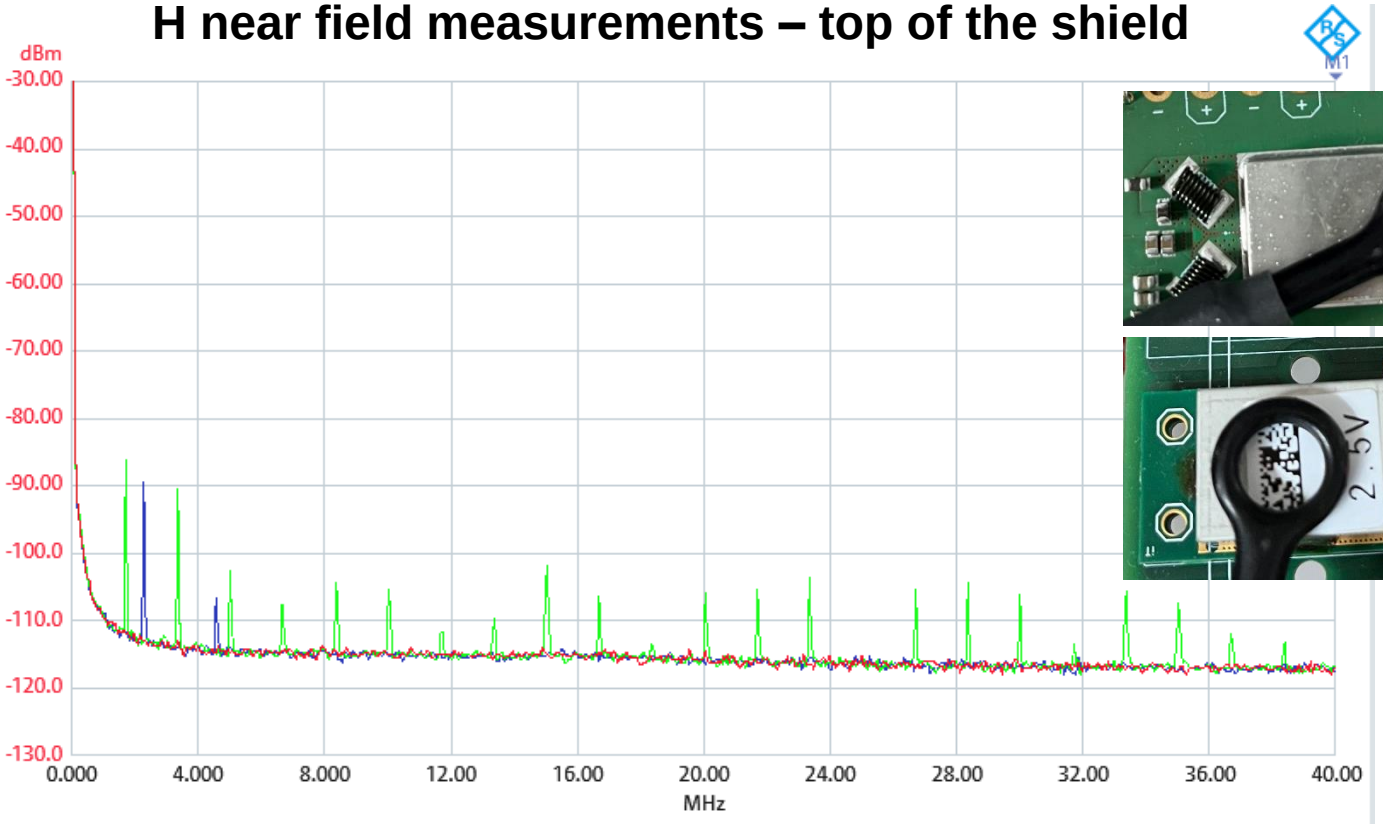
H near field measurements – w/o and with the shield



red – background, blue – LVR card without shield,
green – LVR card with shield

Shielding effectiveness comparison

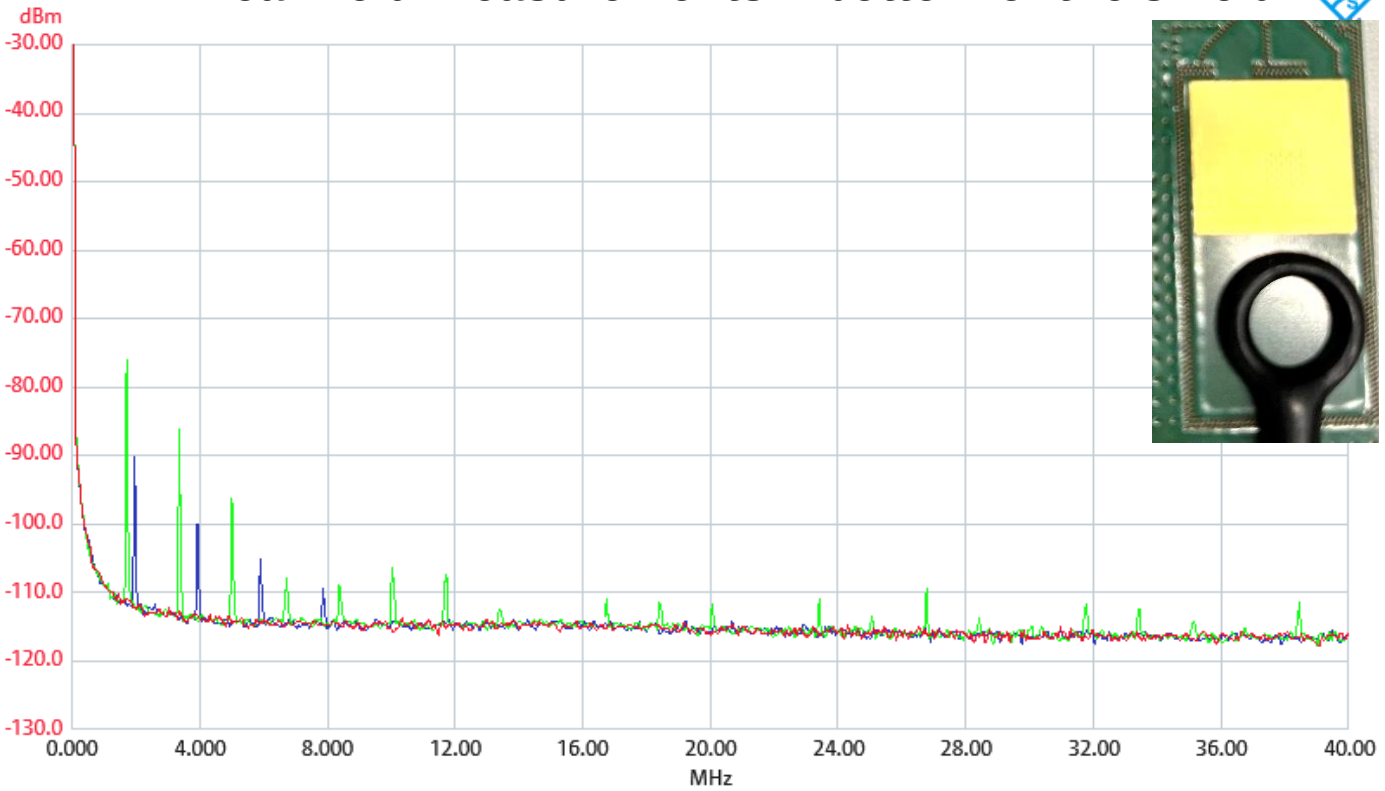
H near field measurements – top of the shield



red – background, blue – LVR card, green – FEASTMP-CLP

Shielding effectiveness comparison

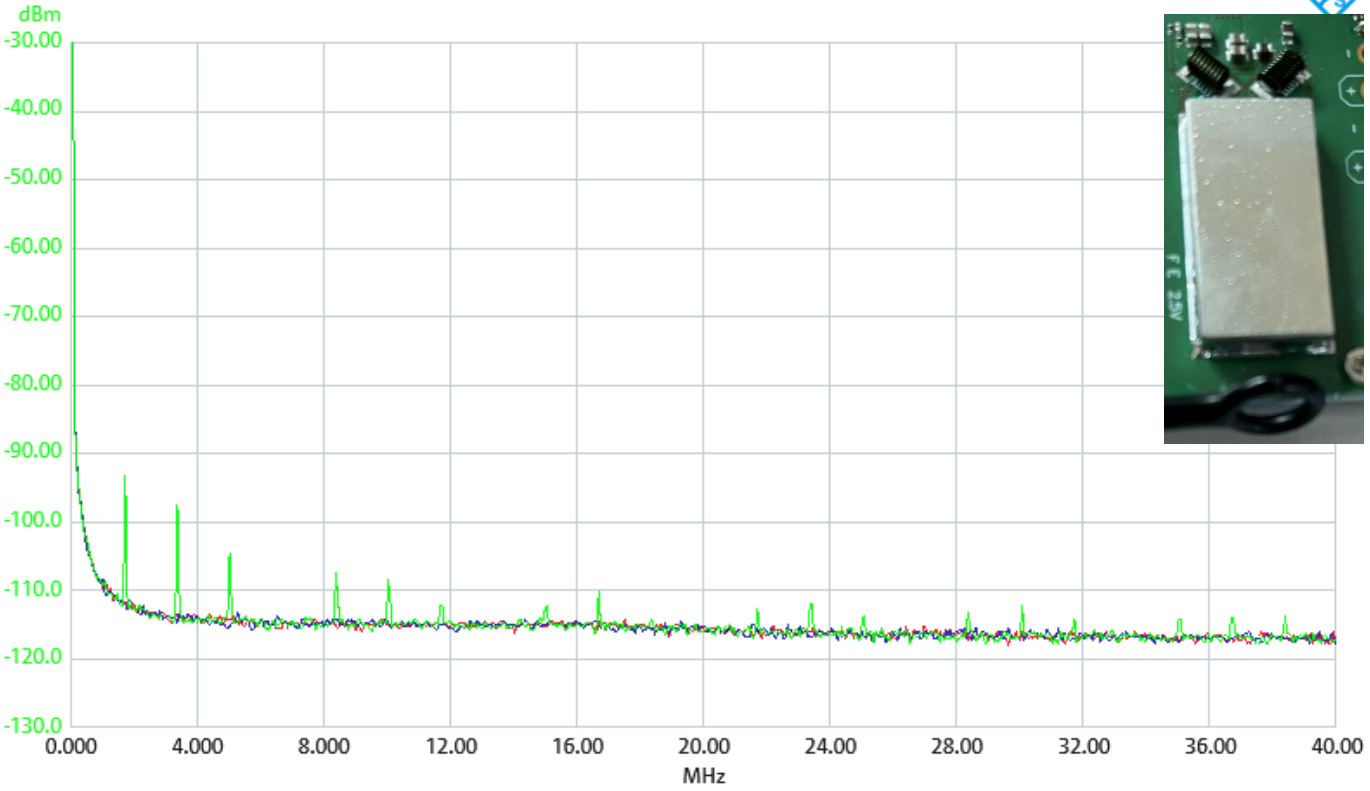
H near field measurements – bottom of the shield



red – background, blue – LVR card, green – FEASTMP-CLP

Shielding effectiveness comparison

H near field measurements – side of the PCB



red – background, blue – LVR card, green – FEASTMP-CLP

Performance

- **The 1.8 V converters on PCC were run at 5.3 A load for a month.**
- **Typical efficiency and load regulation plots measured on PCC card with our test setup:**

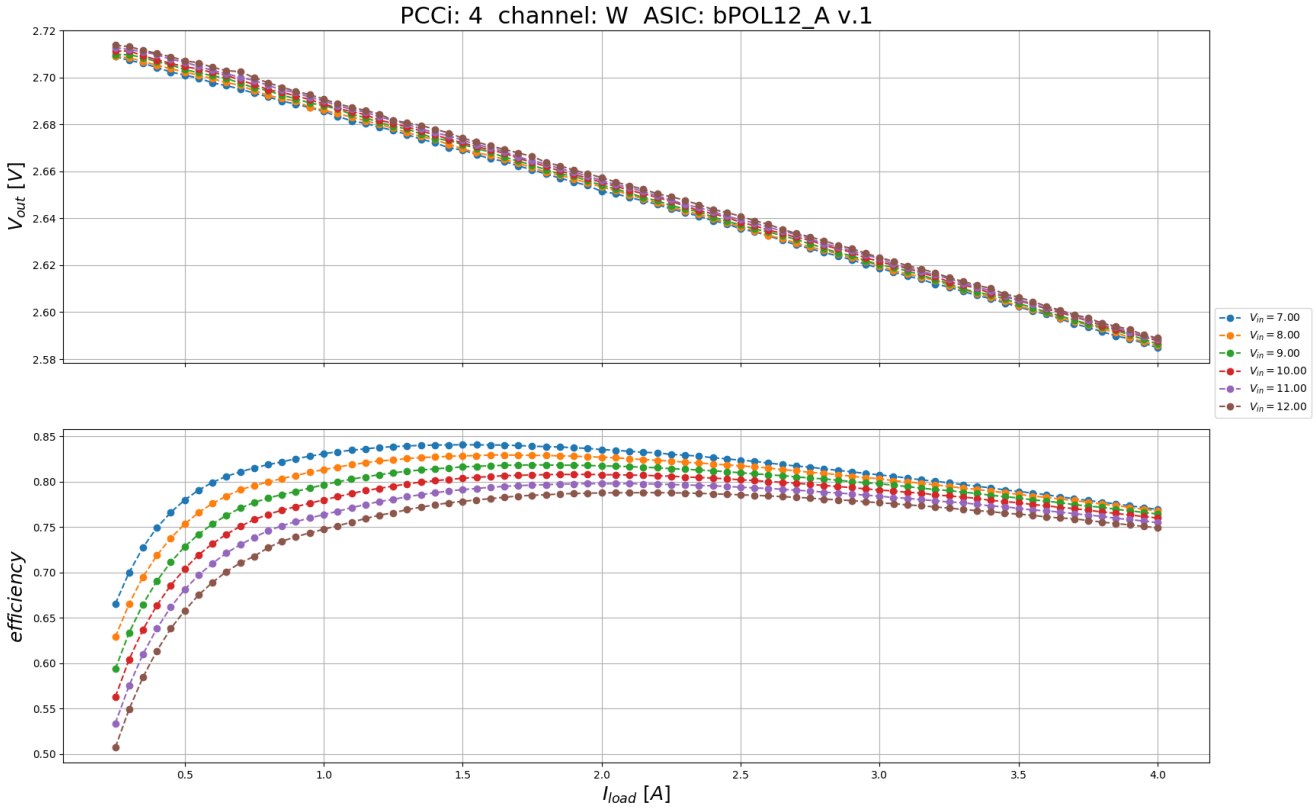


Figure: PCCi4 channel W, efficiency and load regulation plots. Include: output filter, interconnect and fan-out PCB.

Observed features - oscillations

- **Feature observed in specific load conditions, depending on the regulated output voltage (spans as small as 10 mA).**

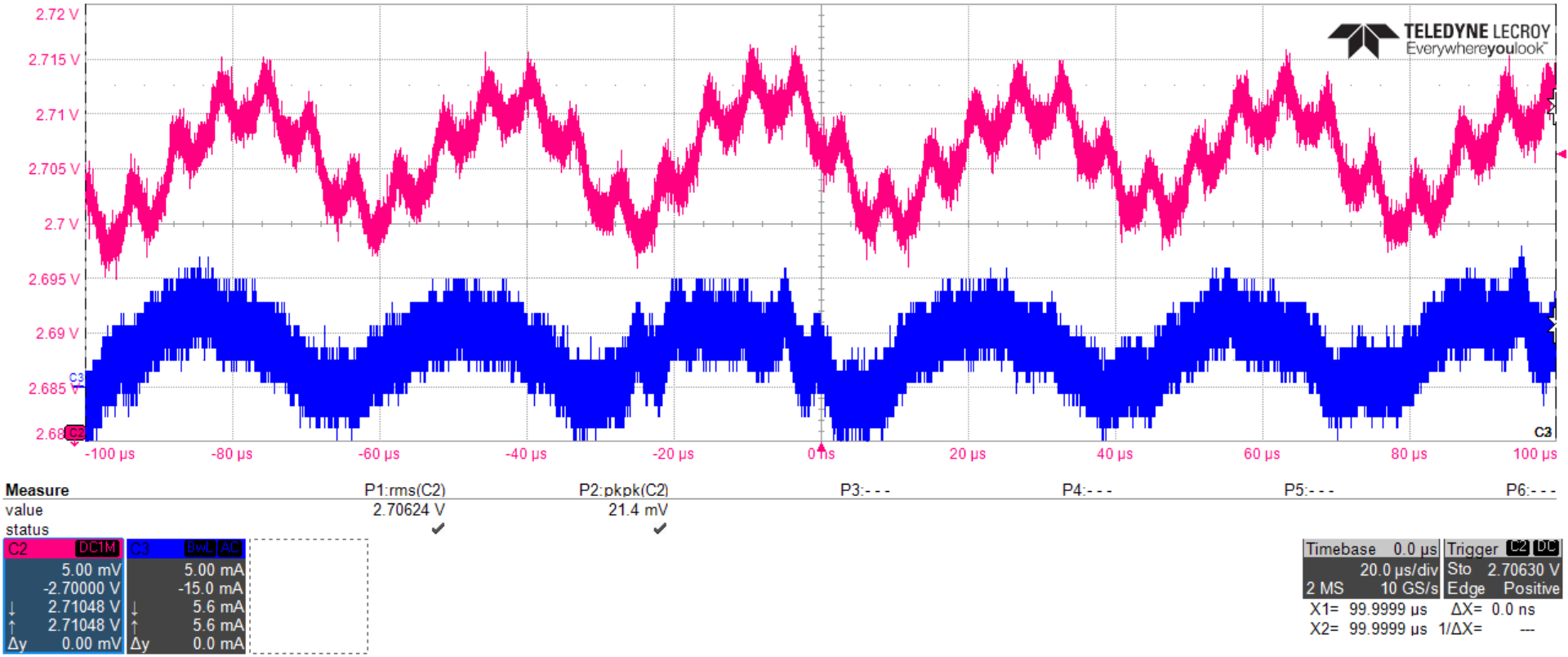


Figure: Oscillation recorded on the PCCi5 card with bPOL regulating 2.7 V; V_{in} = 12 V; A_{out} = 1.0 A. Pink plot - DC coupled output voltage, Blue plot - AC coupled output current.

Observed features - oscillations

- **Feature observed in 9 out of 20 converters for both ASICs.**

Table: Low frequency oscillations measured at the output of the DC-DC converters. Measurements performed with 10 mA step load scan. (green field – no oscillations observed). Current values denote range in which oscillations are present.

input voltage / converter	7 V	8 V	9 V	10 V	11 V	12 V
PCCi1_FEAST_X_1v8	530 – 600 mA 7.5 – 11.2 kHz	560 – 630 mA 8.3 - 11.6 kHz	580 – 650 mA 8.5 – 11.6 kHz	600 – 670 mA 8.7 – 11.7 kHz	620 – 680 mA 9.0 – 11.8 kHz	630 – 700 mA 9.3 – 12.0 kHz
PCCi1_FEAST_Y_1v2						
PCCi1_FEAST_W_2v5						
PCCi1_FEAST_Z_1v8						
PCCi2_FEAST_X_1v8						
PCCi2_FEAST_Y_1v2						
PCCi2_FEAST_W_2v5						
PCCi2_FEAST_Z_1v8			620 - 630 mA 15.8–16.4 kHz	650 – 670 mA 16.4–16.7 kHz	660 – 690 mA 16.4–19.2 kHz	670 – 700 mA 16.2–18.8kHz
PCCi3_bPOL_X_1v8						
PCCi3_bPOL_Y_1v2	500 – 570 mA 19.7–26.5 kHz	510 – 590 mA 19.7-26.3 kHz	520 – 610 mA 19.5–26.5 kHz	530 – 610 mA 20.1–22.2 kHz	540 – 630 mA 20.9–27.5 kHz	550 – 640 mA 21.7–28.5 kHz
PCCi3_bPOL_W_2v5					800 – 810 mA 31.9–41.9 kHz	820 – 850 mA 39.9–42.7 kHz
PCCi3_bPOL_Z_1v8						
PCCi4_bPOL_X_1v8						
PCCi4_bPOL_Y_1v2	410 – 520 mA 15.9–19.9 kHz	420 – 540 mA 16.1-22.9 kHz	420 – 560 mA 16.1–23.5 kHz	420 – 580 mA 16.3–24.6 kHz	430 – 580 mA 16.5–25.6 kHz	430 – 590 mA 16.5–27.4 kHz
PCCi4_bPOL_W_2v5	750 – 800 mA 20.1–27.6 kHz	800 – 870 mA 20.5-28.6 kHz	840 – 920 mA 21.3–30.6 kHz	870 – 950 mA 22.3–28.7 kHz	900–1010 mA 23.3–33.6 kHz	920–1040 mA 23.5–35.3 kHz
PCCi4_bPOL_Z_1v8						
PCCi5_bPOL_X_1v8						
PCCi5_bPOL_Y_1v2	420 – 560 mA 16.0–22.4kHz	430 – 560 mA 16.0–22.6 kHz	440 – 580 mA 16.2–23.6 kHz	440 – 610 mA 15.4–26.9 kHz	450 – 610 mA 16.2–27.2 kHz	450 – 620 mA 15.4–29.3 kHz
PCCi5_bPOL_W_2v5	740 – 840 mA 19.5–31.6kHz	800 – 900 mA 21.3–33.0 kHz	840 – 970 mA 21.9–34.5 kHz	870–1010 mA 22.6–36.3 kHz	900–1060 mA 23.8–38.2 kHz	920–1080 mA 24.2–39.1 kHz
PCCi5_bPOL_Z_1v8	540 – 670 mA 13.8–22.2kHz	560 – 700 mA 14.2–23.4 kHz	590 – 730 mA 15.4–24.9 kHz	610 – 750 mA 16.0–26.4 kHz	620 – 770 mA 16.4–26.9 kHz	630 - 780 mA 16.4–27.6 kHz

Observed features – efficiency drops

- **Feature observed in a very narrow input voltage span of 250-300 mV.**

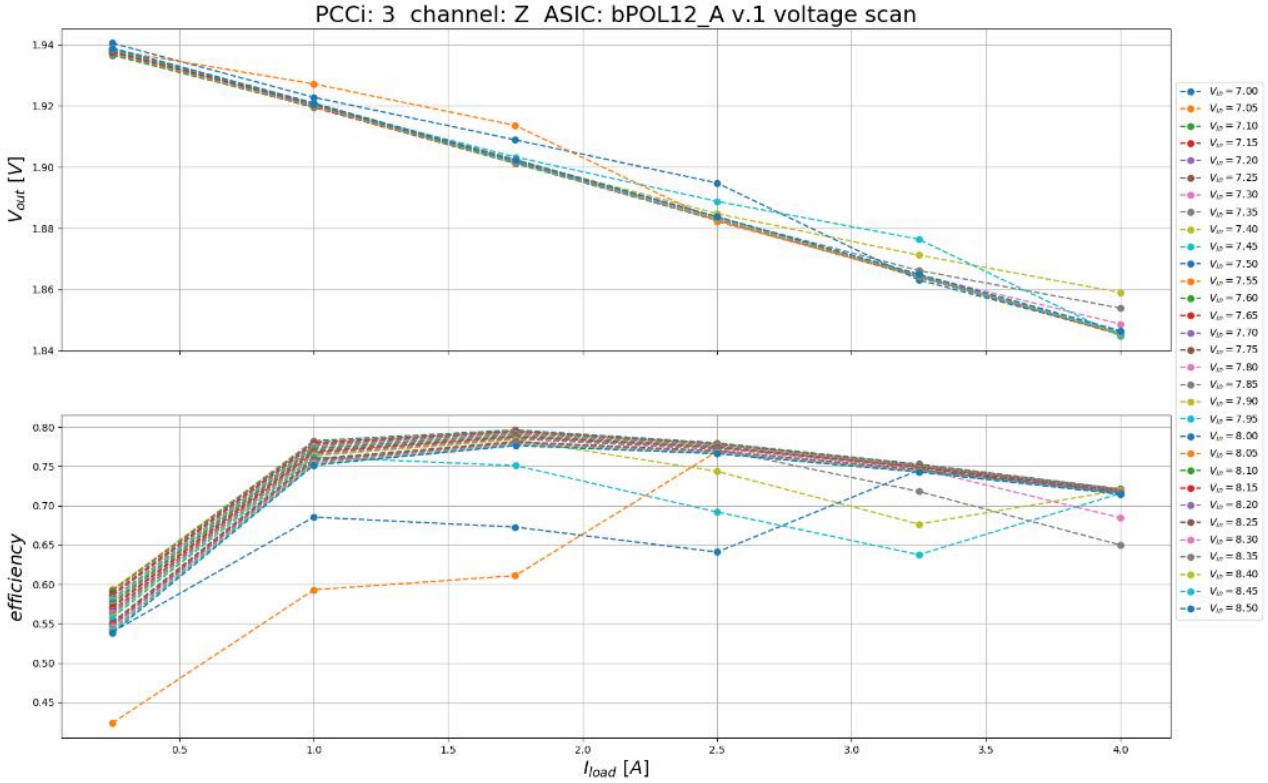


Figure: PCCi3 channel Z, efficiency decrease problem reminder, target plot at V_{in} = 8 V

Observed features – efficiency drops

- **Feature observed in 12 out of 20 converters for bPOLs only:**
  - **FEAST2s has the same problem but outside of our operating range <7 V.**

Table: Input voltage regions causing efficiency drops in DC-DC converters measured at 0.25 – 4 A load (green field - none observed)

input voltage / converter	7 – 8.5 V	8.5 – 10 V	10 – 12 V
PCCi1_FEAST_X_1v8			
PCCi1_FEAST_Y_1v2			
PCCi1_FEAST_W_2v5			
PCCi1_FEAST_Z_1v8			
PCCi2_FEAST_X_1v8			
PCCi2_FEAST_Y_1v2			
PCCi2_FEAST_W_2v5			
PCCi2_FEAST_Z_1v8			
PCCi3_bPOL_X_1v8	8.10 – 8.35 V		
PCCi3_bPOL_Y_1v2	7.95 – 8.20 V		
PCCi3_bPOL_W_2v5	7.95 – 8.25 V		
PCCi3_bPOL_Z_1v8	7.80 – 8.05 V		
PCCi4_bPOL_X_1v8	8.05 – 8.25 V		
PCCi4_bPOL_Y_1v2	8.20 – 8.40 V		
PCCi4_bPOL_W_2v5	8.20 – 8.45 V		
PCCi4_bPOL_Z_1v8	8.15 – 8.40 V		
PCCi5_bPOL_X_1v8	7.00 – 7.25 V		
PCCi5_bPOL_Y_1v2	7.85 – 8.10 V		
PCCi5_bPOL_W_2v5	7.85 – 8.15 V		
PCCi5_bPOL_Z_1v8	7.50 – 7.75 V		

Summary

- More than 14,000 DC-DC converters will be produced and installed in CMS MTD BTL and ECAL barrel during the LHC Long Shutdown 3.
- Design of a common DC-DC conversion block for PCC and LVR cards has matured to a production ready state.
- A discrete solid wire toroid has been selected as the main inductor.
- Several techniques for shielding have been proposed and their effectiveness compared to the existing FEASTMP modules.
- FEAST2 and bPOL12 have been evaluated as the switching ASIC suitable for the application, some features found in both.
- bPOL12 as an in-development ASIC showed better perspectives for the future performance, mostly in voltage stability and possibility of mitigation of the unwanted features.

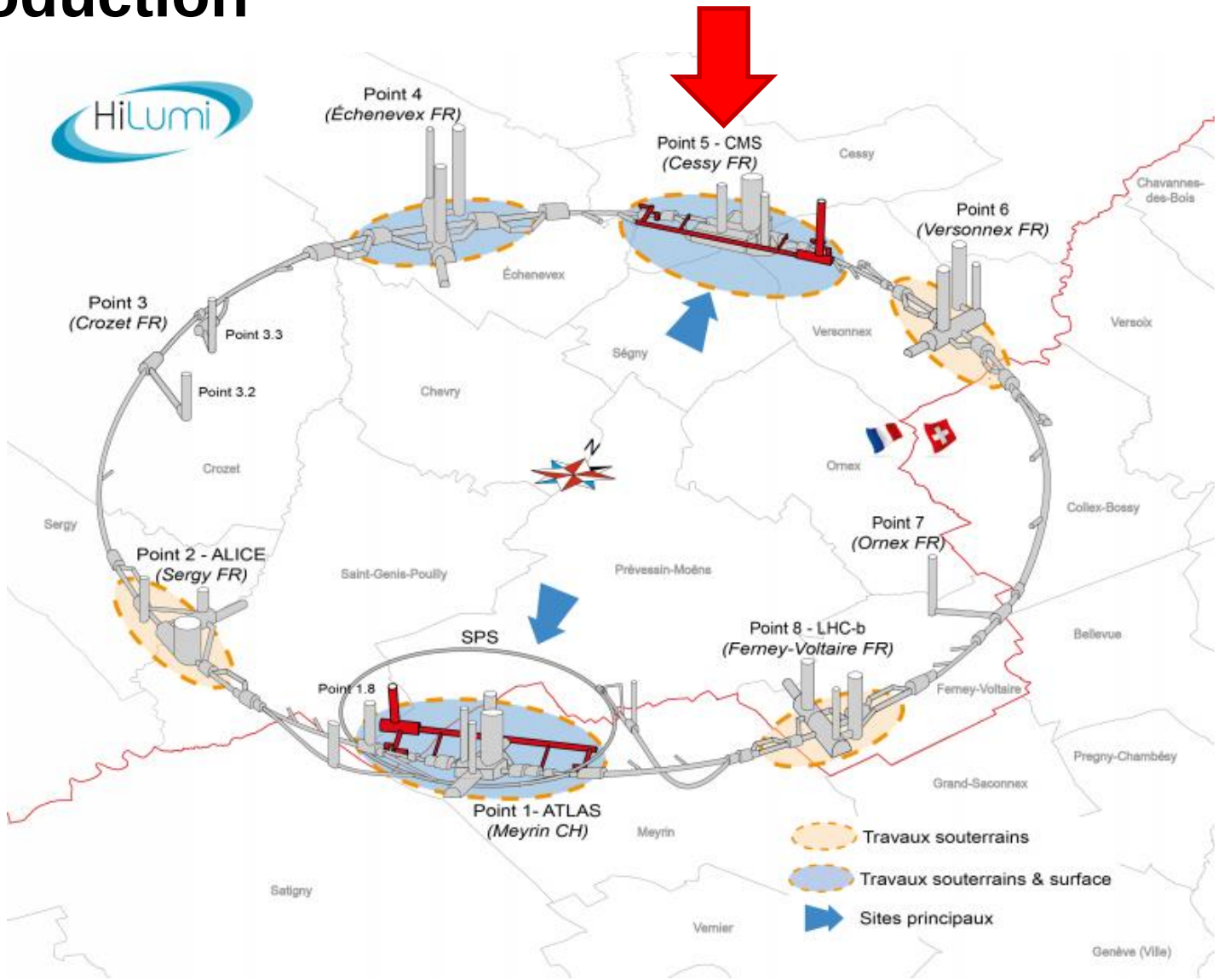
For YOUR attention and the ORGANIZERS for the opportunity to present our work!

This work was supported by the Swiss National Science Foundation with SNF FLARE grant 201476.

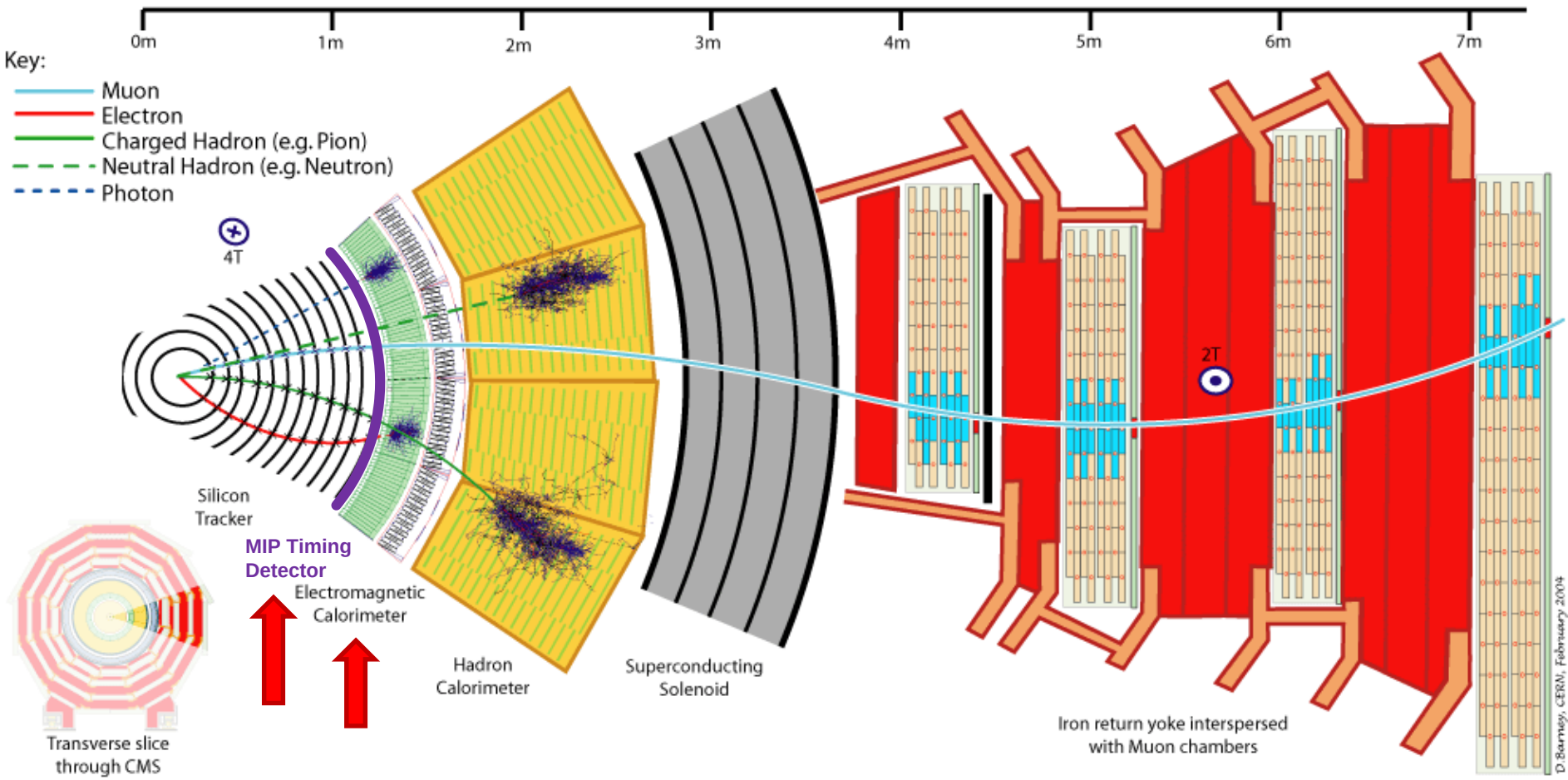
Back-up Slides

Back-up Slides

Introduction



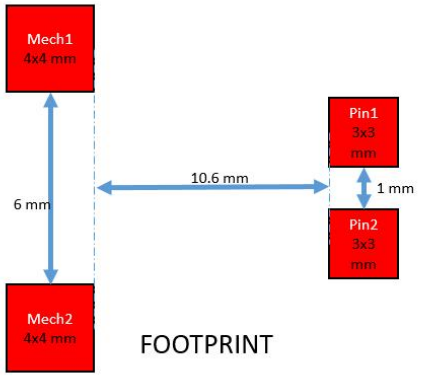
Introduction



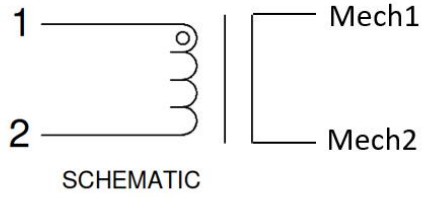
Main inductor specification

MECHANICAL SPECIFICATIONS

Physical parameters [mm or unitless]		
Dimension	Minimum	Maximum
Length	17.2	17.7
Width	13.8	14.2
Height	4.4	4.7
Flatness	0.15	0.25
Leads pitch (pin 1-2)	3.5	4.5
Number of windings	33	35
Suction pad diameter	10	14
Suction pad thickness	0.25	0.5

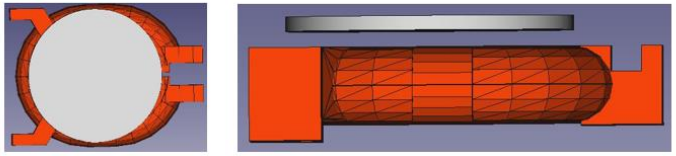


FOOTPRINT



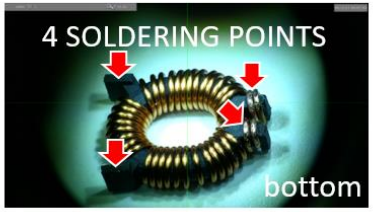
SCHEMATIC

SUCTION PAD MODEL



EXEMPLE OF BOBBIN SOLDERING FEET

TOROID PROTOTYPE PICTURES



ELECTRICAL SPECIFICATIONS

Inductance pins 1-2 [nH]		
Frequency	Minimum	Maximum
10 kHz	480	510
100 kHz	450	490
1.8 MHz	410	450
3 MHz	400	440

DC Resistance [Ω]		
	Minimum	Maximum
Pins 1-2	0.02	0.027
Pins 1-3	10^6	
Pins 1-4	10^6	
Pins 2-3	10^6	
Pins 2-4	10^6	
Pins 3-4	10^6	

ETH toroidal inductor 470nH@100kHz

Shielding – near field

total shielding effectiveness: $S = A + R + B\ [dB]$

absorption loss: $A = 131.5t\sqrt{f\mu_r\sigma_r}\ [dB]$

electric field reflection loss: $R_e = 322 + 10\log\frac{\sigma_r}{\mu_r f^3 r^2}\ [dB]$

magnetic field reflection loss: $R_m = 14.6 + 10\log\left(\frac{fr^2\sigma_r}{\mu_r}\right)\ [dB]$

correction factor for multiple reflections: $B = 20\log\left(1 - e^{-\frac{2t}{\delta}}\right)\ [dB]$

t − thickness, r − distance from source, μ_r − *relative permeability*, σ_r − *relative (to Cu) conductivity*, f − *frequency*, δ − *skin depth* $\left\{\frac{0.066}{\sqrt{f\mu_r\sigma_r}}\ [m]\right\}$

from *Electromagnetic compatibility engineering*, **H. W. Ott**

Shielding – near field

total shielding effectiveness: $S = A + R + B\ [dB]$

absorption loss: $A = 131.5t\sqrt{f\mu_r\sigma_r}\ [dB]$

Shield parameters selection

- Converters operate in 3.8 T field therefore shield's relative permeability should be close to 1
- Frequency is given by an external resistor (1-3 MHz)
- Remaining factors to play with: **conductivity, thickness and size**

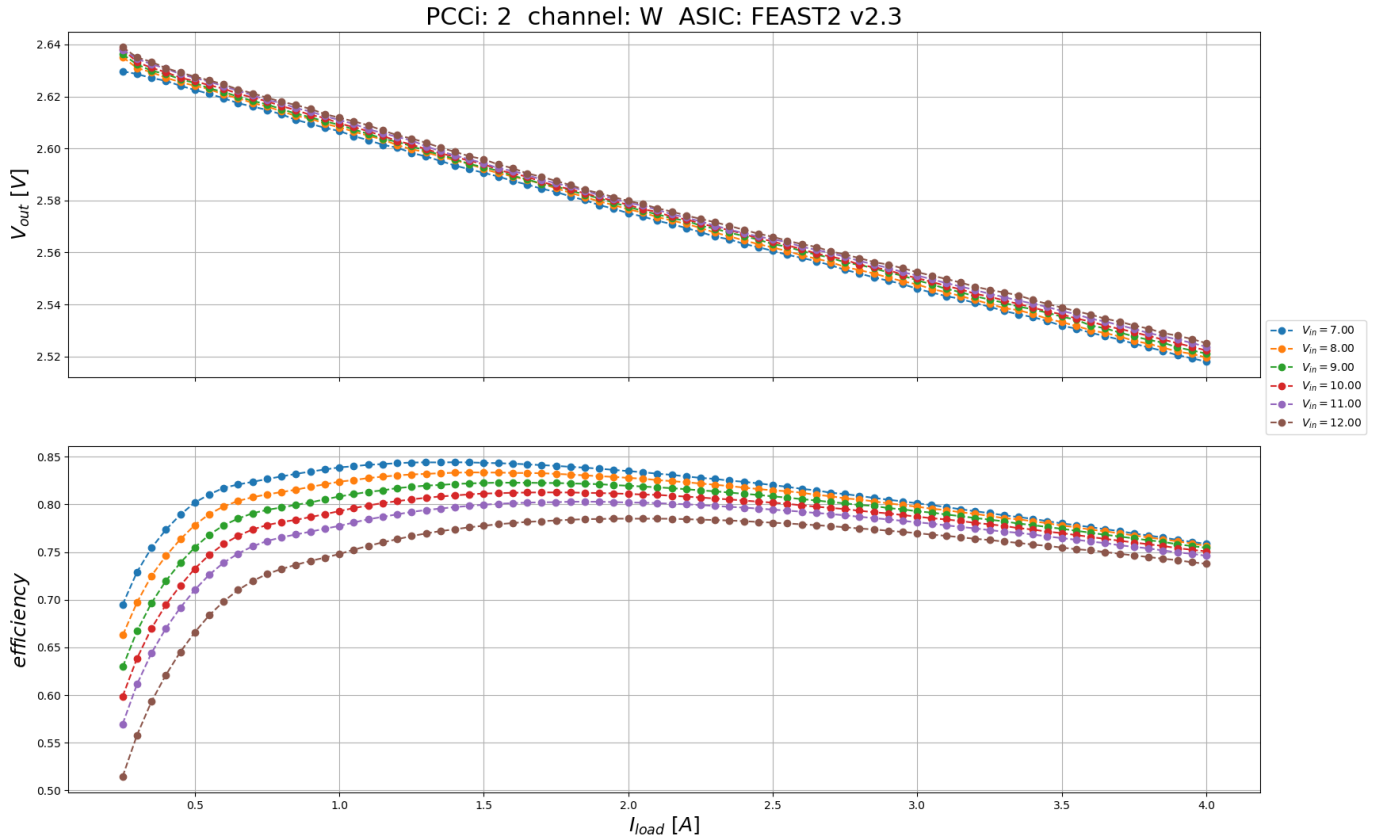
- In BTL and ECAL case 300 um copper has been selected (-53 dB absorption both on paper and measured)
- Thin tin plating advisible for better soldering, but not too much

correction factor for multiple reflections: $B = 20\log(1 - e^{-\delta})\ [dB]$

t − thickness, r − distance from source, μ_r − *relative permeability*,
σ_r − *relative (to Cu) conductivity*, f − *frequency*, δ − *skin depth* $\left\{\frac{0.066}{\sqrt{f\mu_r\sigma_r}}\ [m]\right\}$

from *Electromagnetic compatibility engineering*, **H. W. Ott**

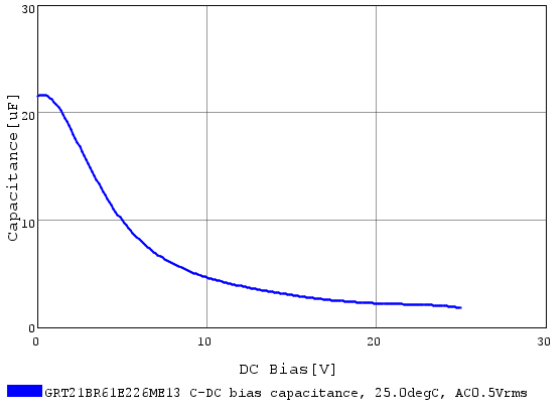
Performance



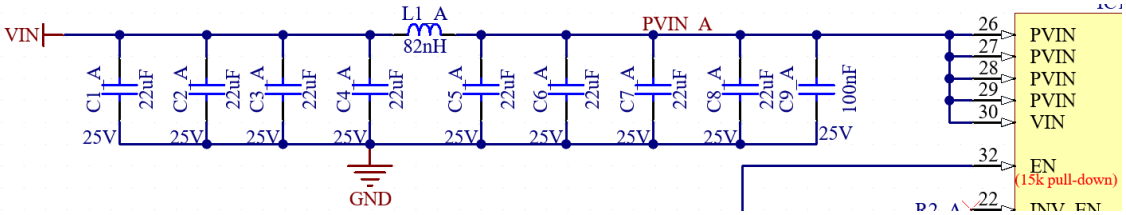
Implementation - Input filter

- **Input filter design:**
  - **Passive PI filter, with 82 nH inductor (better separation of multiple converters).**
  - **Follows the recommendations from ASIC's datasheet of at least 20 µF bulk capacitance and a low ESL capacitor placed next to the ASIC input.**
  - **Because of the C-DC characteristics of the MLCCs there is a need for several parallel components.**

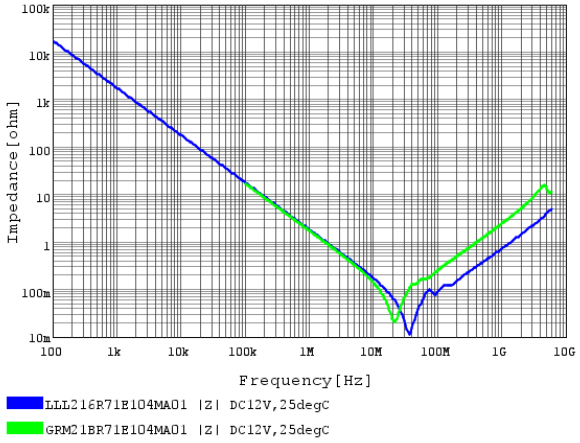
Ferroelectric properties of MLCC



Schematic of the input filter implemented in the DC-DC converters.

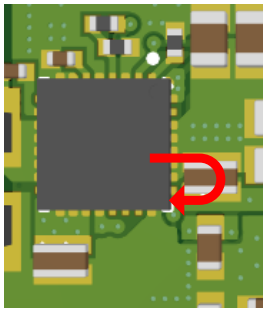


Low ESL MLCC (inverted geometry)

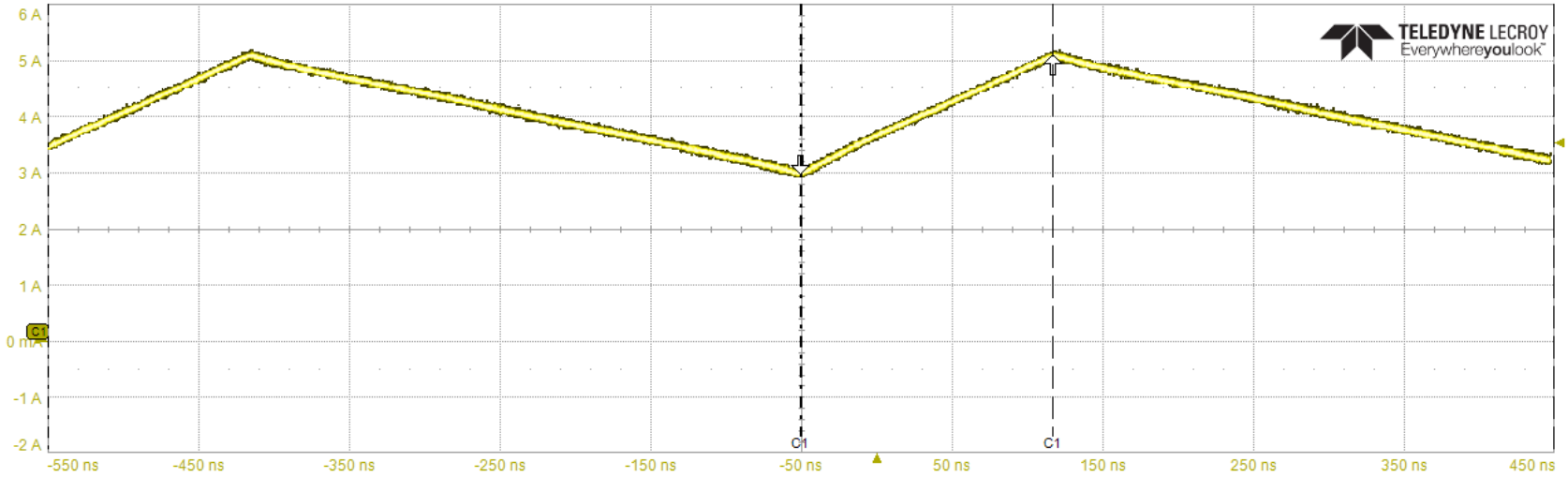


Input inductance consideration

- **Low ESL input capacitor:**
  - **The capacitor is placed as close as possible to the ASIC input.**
  - **Simulation of loop inductance showed <400pH including wire bonds of the ASIC, voltage induced while switching:**



$$V = -L\frac{di}{dt} = -0.4\,nH\,\frac{2.23\,A}{161\,ns} \approx -5.54\,mV$$

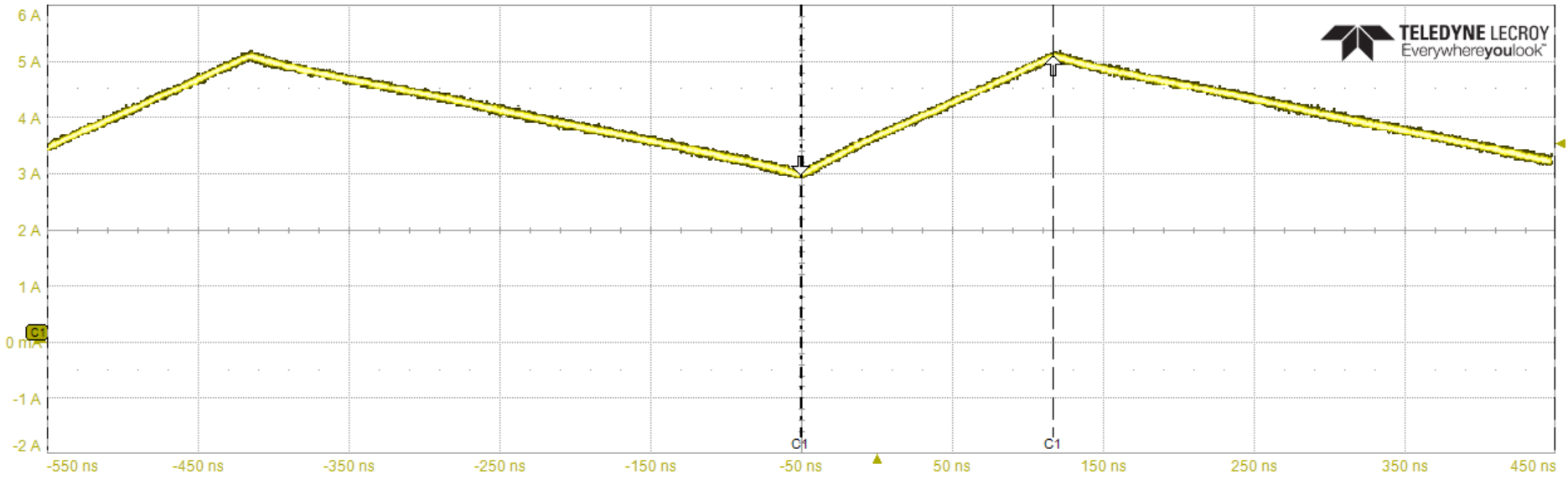


Current through main inductor measured with 30A 100 MHz probe

Input inductance consideration

$$dq = \int di(t)dt = \frac{2.23\ A\ \cdot 161\ ns}{2} = 179.5\ nC$$

$$dV = \frac{dq}{C} = \frac{179.5\ nC}{100\ nF} = 1.795\ V$$



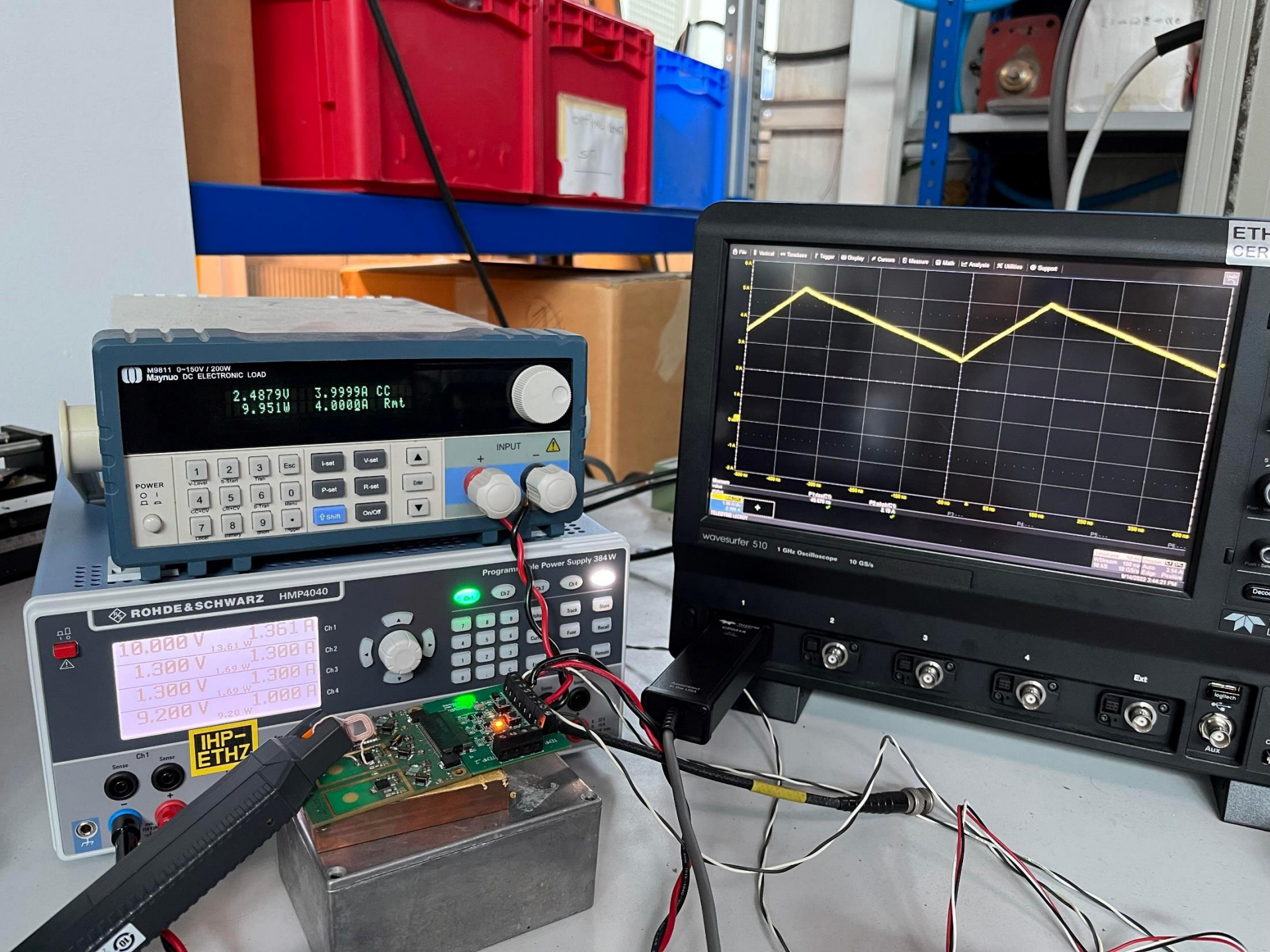
Measure	P1:rise(C1)	P2:pkpk(C1)	P3:- - -	P4:- - -	P5:- - -	P6:- - -
value	137.595 ns	2.23 A				
status		✔				

C1 BwL DC
1.00 A/div
-2.000 A
↓ 2.963 A
↑ 5.055 A
Δy 2.138 A

Timebase 50 ns
WStream 100 ns
10 kS 10 GS/s

Trigger C1 DC
Auto 3.54 A
Edge Positive

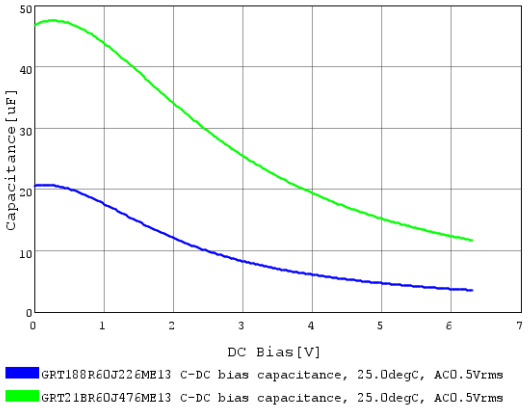
X1= -50.2 ns ΔX= 167.1 ns
X2= 116.9 ns 1/ΔX= 5.984 MHz

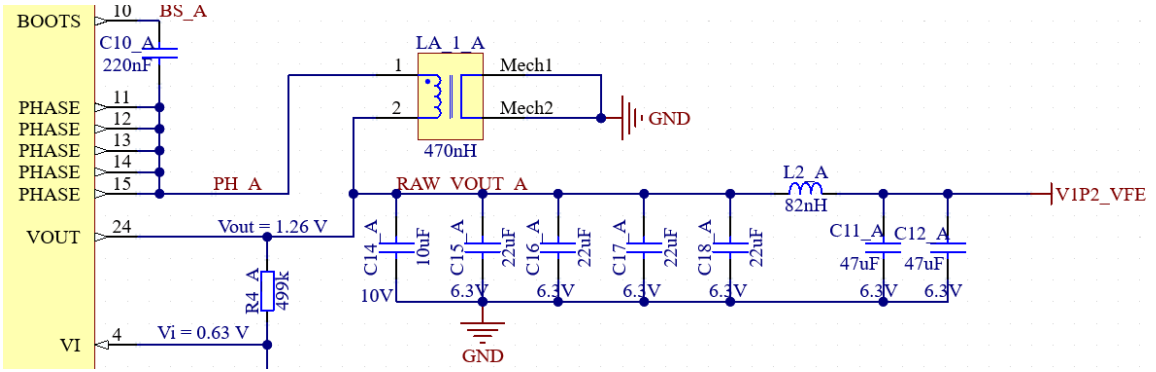

M9811 0~150V / 200W
Maynuo DC ELECTRONIC LOAD
2.4879V 3.9999A CC
9.951W 4.0000A Rmt
INPUT
ROHDE&SCHWARZ HMP4040
10.000 V 1.361 A
1.300 V 1.300 A
1.300 V 1.300 A
9.200 V 1.000 A
IHP-ETHZ
wavesurfer 510 1 GHz Oscilloscope 10 GS/s

Implementation - Output filter

- **Output filter design:**
  - **Passive PI filter with 82 nH inductor**
  - **Because of the C-DC characteristics of the MLCCs there is a need for several parallel components**

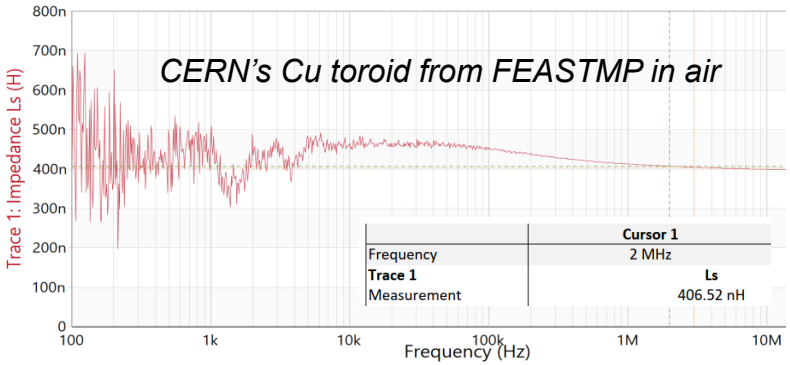
Ferroelectric properties of MLCC



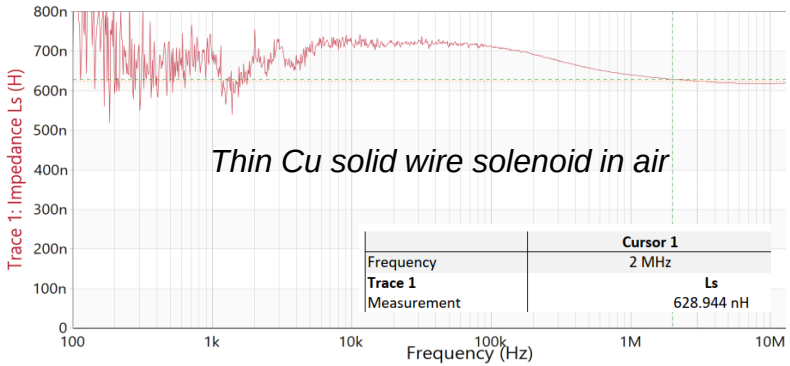


Main inductor - solenoid

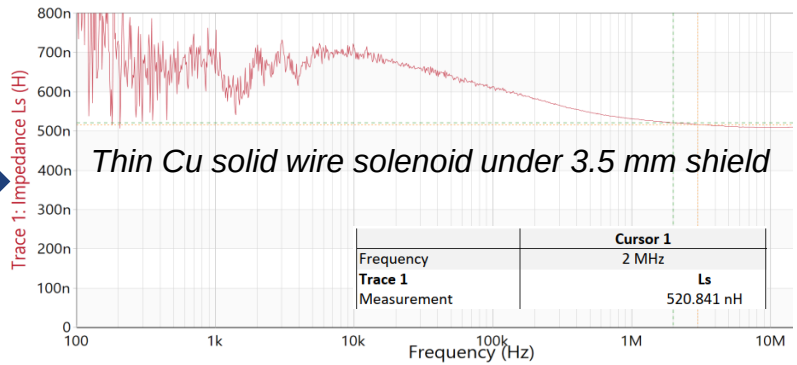
Reference



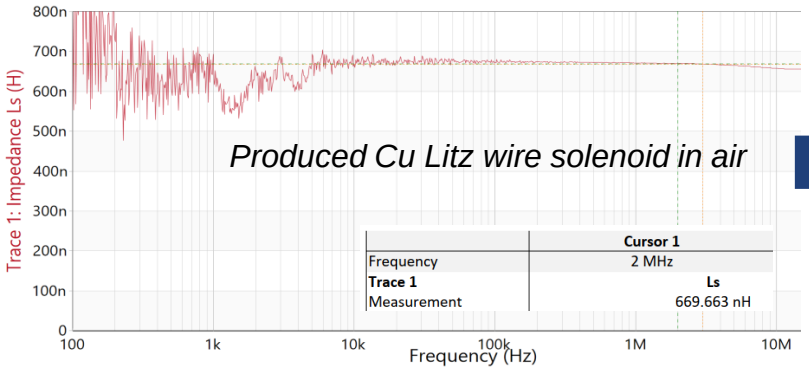
Initial tests



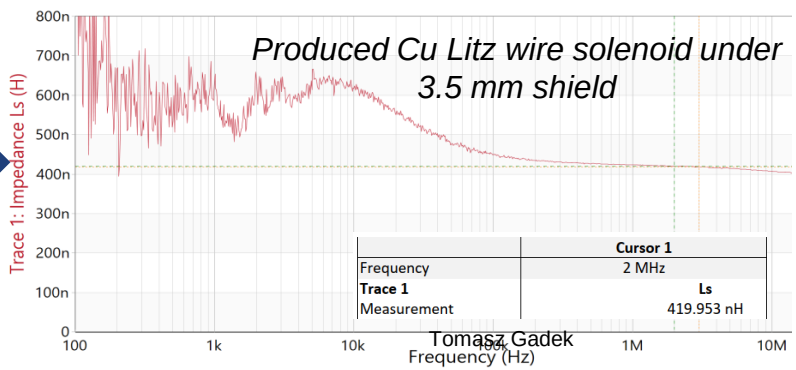
- 17%



Produced prototype



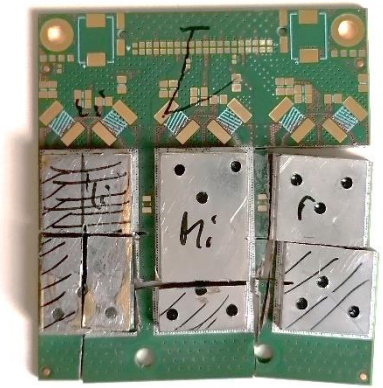
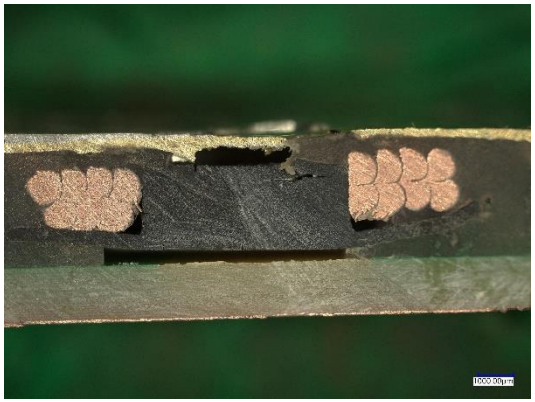
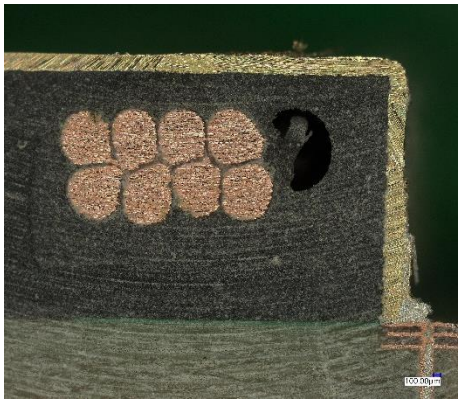
- 37%

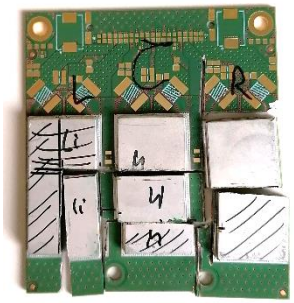
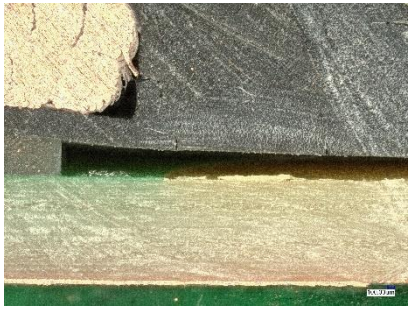
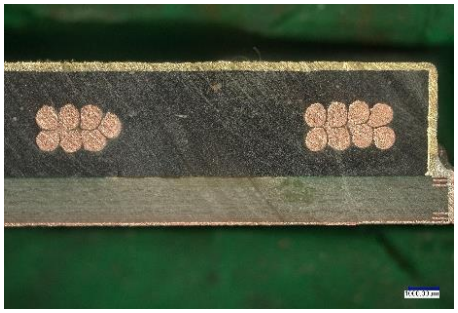
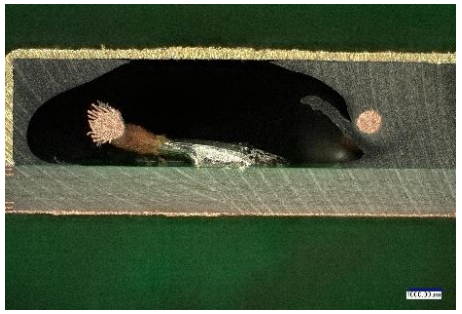


- **Produced coil measurements outcome:**
  - Bigger L drop under shield than anticipated,
  - Final L comparable to FEASTMP toroid (420 vs 406 nH @ 2 MHz)
  - Ok from FEAST designers for L >400 nH
  - Problem understood and "quickest" improvements implemented

Main inductor - solenoid

- **A solenoid in CMS magnet:**
  - DC-DC converters are placed inside of a 3.8 T magnetic field
  - The converter switches at 2 MHz, its oscillating field interacts with CMS magnetic field
  - Potential of mechanical vibrations of the coil
  - To dampen vibrations an encapsulation of the shield cavity needed
  - Cross-sections from encapsulation tries are displayed below:

Environment in CMS EBUP and MTD BTL

Table : Environmental conditions expected in the MTD BTL project

Expected radiation levels	
Fluence	1.90×10^{14} n_{eq}/cm^2
Total Dose	32 kGy
Requested radiation tolerance of components	
Fluence	2.85×10^{14} n_{eq}/cm^2
Total Dose	48 kGy
Temperature levels	
Coolant temperature	-35°C
Requested operating temperature range	-40°C to +60°C
Magnetic Field	
Magnetic field strength	3.8 T

OK

OK

OK

Table 4: Environmental conditions expected in the EBUP project

Expected radiation levels	
Fluence	Smaller than BTL (see Table 1)
Total Dose	Smaller than BTL (see Table 1)
Requested radiation tolerance of components	
Fluence	Smaller than BTL (see Table 1)
Total Dose	Smaller than BTL (see Table 1)
Temperature levels	
Coolant temperature	+8°C
Requested operating temperature range	0°C to +60°C
Magnetic Field	
Magnetic field strength	3.8 T

DC-DC regulation in CMS EBUP and MTD BTL

EBUP

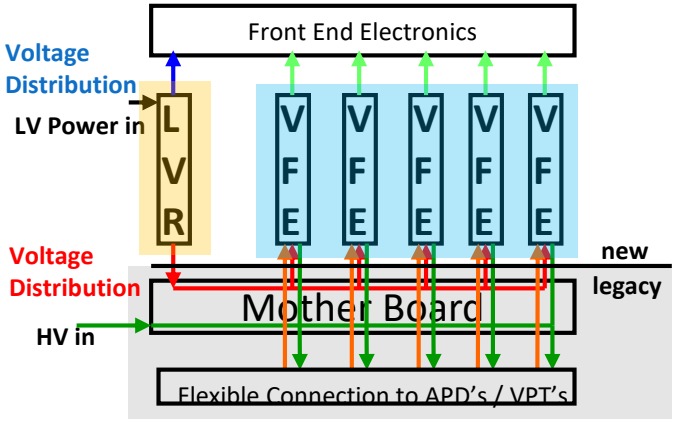


Table: On-detector low voltage distribution and regulation in the EBUP project.

Input voltage	Power distribution	Power conversion		Max. interconnection Resistance at 20°C	Voltage at load	Load current
12 V	READOUT TOWER	LVR	DC-DC-A	40 mΩ	2.5 V	1.5 A
			DC-DC-B	40 mΩ	1.2 V	2.0 A
			DC-DC-C	40 mΩ	2.5 V	1.0 A
			DC-DC-D	40 mΩ	1.2 V	1.4 A
			DC-DC-E	30 mΩ	1.2 V	2.0 A
			DC-DC-F	30 mΩ	2.5 V	1.0 A

MTD BTL

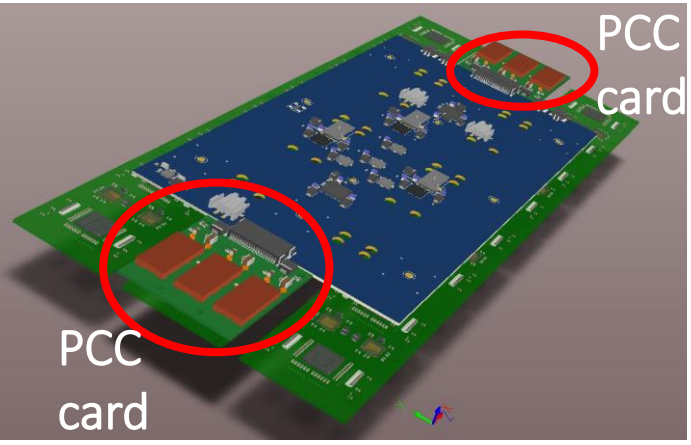
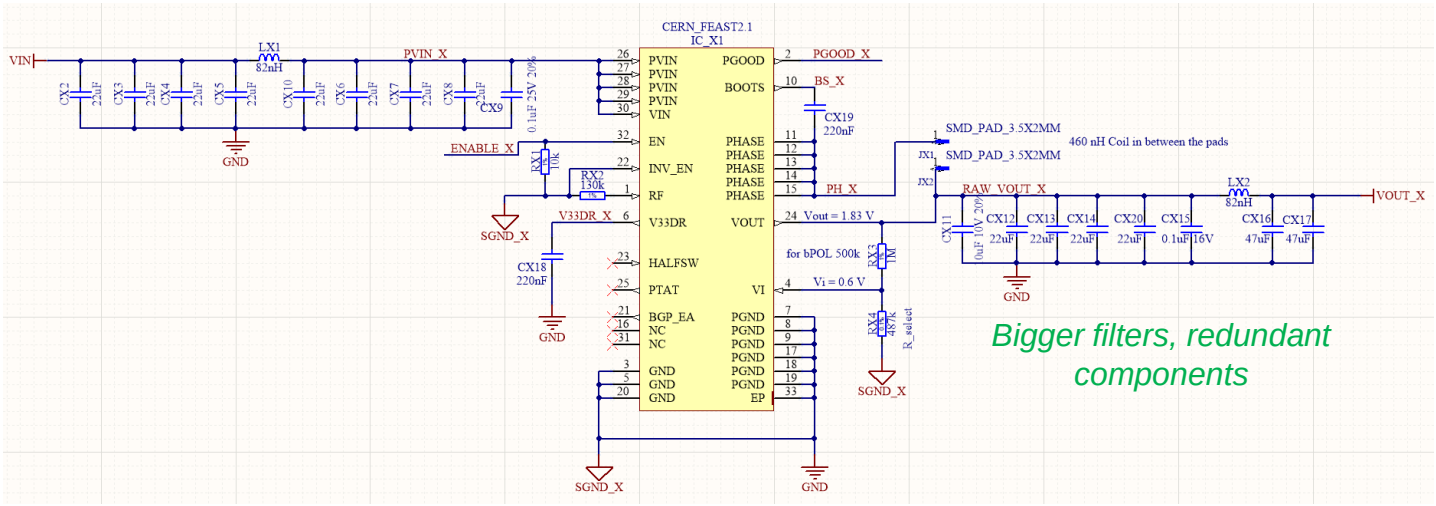


Table: On-detector low voltage distribution and regulation in the MTD BTL project.

Input voltage	Power distribution	Power conversion		Max. interconnection Resistance at 20°C	Voltage at load	Load current
12 V	READOUT UNIT	PCC_L	DC-DC-X	30 mΩ	1.8 V	3.6 A
			DC-DC-Y	30 mΩ	1.2 V	1.2 A
			DC-DC-Z	30 mΩ	1.8 V	3.6 A
		PCC_R	DC-DC-X	30 mΩ	1.8 V	3.6 A
			DC-DC-W	30 mΩ	2.5 V	0.4 A
			DC-DC-Z	30 mΩ	1.8 V	3.6 A

DC-DC regulation in CMS EBUP and MTD BTL



Bigger filters, redundant components

Photo of the top side PCCi v1

Figure: Schematic of a DC-DC converter on the PCC card for MTD BTL project.

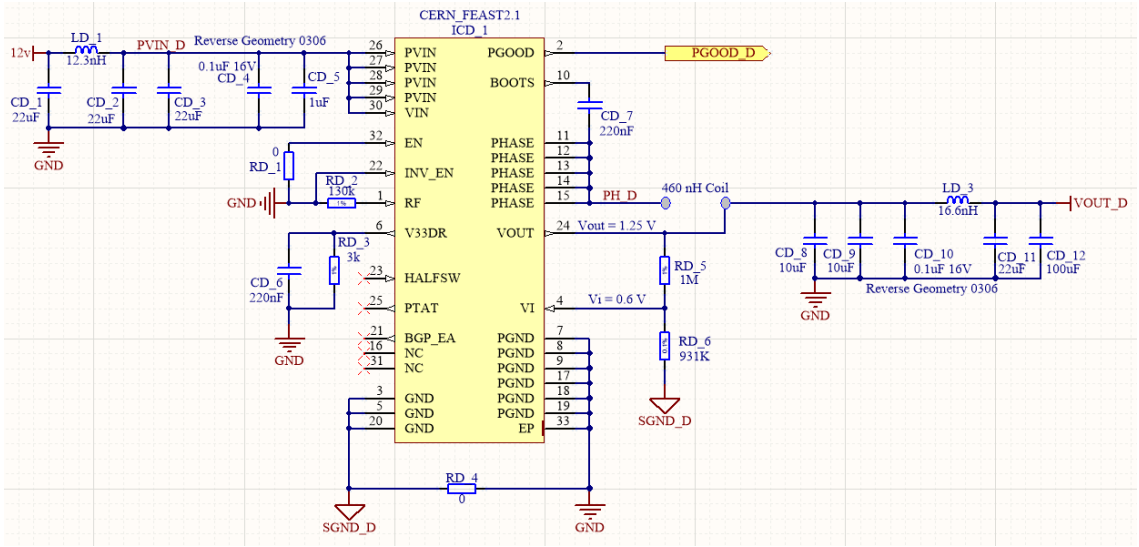


Figure: Schematic of a DC-DC converter on the LVR card for EBUP project.

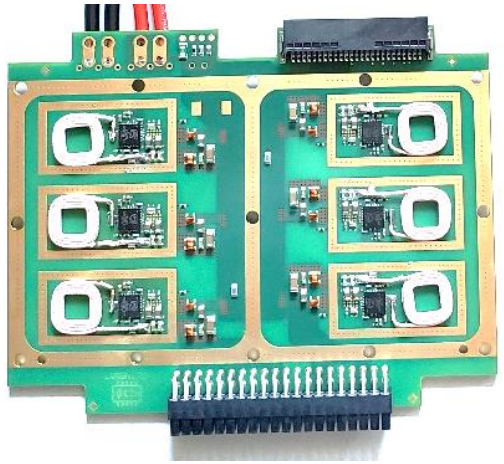


Photo of the top side of LVR

Considerations for output voltage variations

Table: Estimated total output voltage drift for a converter at zero load for both projects.

Configuration	ΔV_{ref_prod}	ΔV_{ref_temp}	ΔV_{ref_rad}	$\Delta R_{ref}/\Delta R_{sel}$	Total drift
bPOL in MTD BTL at -35°C	+0.33% -0.33%	-1.045%	+1.59%	+1.005% -0.995%	1.88% -0.78%
bPOL in MTD BTL at +60°C	+0.33% -0.33%	0.760%	+0.40%	+1.005% -0.995%	2.50% -0.17%
FEAST in MTD BTL at -35°C	+2.34% -2.67%	-1.045%	+1.59%	+1.005% -0.995%	3.89% -3.12%
FEAST in MTD BTL at +60°C	+2.34% -2.67%	0.760%	+0.40%	+1.005% -0.995%	4.51% -2.51%
bPOL in EBUP at +8°C	+0.33% -0.33%	-0.228%	+0.40%	+1.005% -0.995%	1.51% -1.15%
bPOL in EBUP at +60°C	+0.33% -0.33%	0.760%	+0.40%	+1.005% -0.995%	2.50% -0.17%
FEAST in EBUP at +8°C	+2.34% -2.67%	-0.228%	+0.40%	+1.005% -0.995%	3.52% -3.49%
FEAST in EBUP at +60°C	+2.34% -2.67%	0.760%	+0.40%	+1.005% -0.995%	4.51% -2.51%

OK

Considerations for output voltage variations - details

Table: Regulated voltage variations due to production spread

Source of variation	(MIN – μ)/μ	–σ / μ	σ / μ	(MAX – μ)/ μ
Internal reference voltage production spread FEAST	-2.67%*	-0.95%*	0.95%*	2.34%*
Internal reference voltage production spread bPOL	-0.33%**	-0.33%**	0.33%**	0.33%**
Resistors precision	-0.5%	-0.1%	+0.1%	+0.5%
Feedback voltage precision	-0.995%	-0.1998%	+0.2002%	+1.005%
CORNERS FEAST:	-3.67%	-1.15%	1.15%	3.35%
CORNERS bPOL:	-1.33%	-0.53%	0.53%	1.34%

**values taken from an e-mail correspondence with ASIC designers (600±2 mV @ room temperature)
*taken from FEAST2.1 datasheet

Table: Regulated voltage variations due to radiation

Source of variation	σ / μ
Radiation induced voltage drift at -25°C (0 to 5 Mrad)*	+1.59 %
Radiation induced voltage drift at +25°C (0 to 5 Mrad)*	+0.40 %
WORST CORNER FEAST:	1.59%

*values taken from FEASTMP module datasheet for pre version 2 FEAST

Table: Regulated voltage variations due to temperature change

Source of variation	
Vref drift with temperature in bPOL (+15mV from -30 to 100°C)*	+0.019%/°C

*values taken from an e-mail correspondence with ASIC designers

Measurements – Efficiency

Table: Measured efficiencies for DC-DC converters placed on PCC cards under load conditions expected in CMS BTL project.

input voltage / converter	7 V	8 V	9 V	**10 V**	11 V	12 V	MEAN	SD
PCCi1_FEAST_X_1v8 @ 3.6 A	73.47%	73.05%	72.60%	**71.99%**	71.35%	70.61%	72.18%	1.08%
PCCi1_FEAST_Z_1v8 @ 3.6 A	73.01%	72.68%	72.24%	**71.73%**	71.16%	69.71%	71.76%	1.20%
PCCi2_FEAST_X_1v8 @ 3.6 A	73.21%	72.74%	72.14%	**71.55%**	70.88%	70.15%	71.78%	1.15%
PCCi2_FEAST_Z_1v8 @ 3.6 A	73.65%	73.25%	72.76%	**72.10%**	71.47%	70.30%	72.26%	1.24%
PCCi3_bPOL_X_1v8 @ 3.6 A	72.22%	71.63%	70.92%	**70.17%**	69.35%	68.46%	70.46%	1.41%
PCCi3_bPOL_Z_1v8 @ 3.6 A	73.58%	73.10%	72.55%	**71.79%**	71.05%	70.20%	72.05%	1.28%
PCCi4_bPOL_X_1v8 @ 3.6 A	71.54%	72.42%	71.83%	**71.07%**	70.35%	69.55%	71.13%	1.04%
PCCi4_bPOL_Z_1v8 @ 3.6 A	73.61%	73.03%	72.35%	**71.63%**	70.84%	70.02%	71.91%	1.35%
PCCi5_bPOL_X_1v8 @ 3.6 A	72.99%	72.43%	71.88%	**71.12%**	70.34%	69.51%	71.38%	1.31%
PCCi5_bPOL_Z_1v8 @ 3.6 A	73.82%	73.38%	72.73%	**72.05%**	71.28%	70.49%	72.29%	1.27%
PCCi1_FEAST_Y_1v2 @ 1.2 A	73.18%	71.16%	69.12%	**67.08%**	65.08%	60.27%	67.65%	4.61%
PCCi2_FEAST_Y_1v2 @ 1.2 A	73.71%	71.75%	69.69%	**67.67%**	65.63%	61.85%	68.38%	4.29%
PCCi3_bPOL_Y_1v2 @ 1.2 A	73.04%	70.91%	68.73%	**66.62%**	64.50%	62.41%	67.70%	3.98%
PCCi4_bPOL_Y_1v2 @ 1.2 A	73.05%	70.88%	68.73%	**66.59%**	64.48%	62.37%	67.68%	4.00%
PCCi5_bPOL_Y_1v2 @ 1.2 A	73.24%	70.96%	68.88%	**66.72%**	64.61%	62.51%	67.82%	4.00%
PCCi1_FEAST_W_2v5 @ 0.4 A	76.61%	73.75%	71.17%	**68.65%**	66.17%	59.56%	69.32%	6.03%
PCCi2_FEAST_W_2v5 @ 0.4 A	77.35%	74.60%	71.98%	**69.48%**	67.00%	62.12%	70.42%	5.47%
PCCi3_bPOL_W_2v5 @ 0.4 A	75.02%	72.01%	69.21%	**66.50%**	63.96%	61.55%	68.04%	5.04%
PCCi4_bPOL_W_2v5 @ 0.4 A	74.93%	71.87%	69.05%	**66.37%**	63.81%	61.36%	67.90%	5.07%
PCCi5_bPOL_Y_2v2 @ 0.4 A	75.29%	72.31%	69.47%	**66.79%**	64.21%	61.79%	68.31%	5.05%

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Measurements – Line regulation

Table: Measured output voltage evolution for DC-DC converters placed on PCC cards under load conditions expected in CMS BTL project. Line regulation (last column) calculated based on presented measurements.

input voltage / converter	7 V	8 V	9 V	**10 V**	11 V	12 V	MEAN	**SD**	**$\Delta V_o/V_o/\Delta V_i$**
PCCi1_FEAST_X_1v8 @ 3.6 A	1.8270	1.8278	1.8293	1.8305	1.8314	1.8326	1.8298	**0.0021**	0.06 %/V
PCCi1_FEAST_Z_1v8 @ 3.6 A	1.6865	1.6877	1.6881	1.6891	1.6903	1.6909	1.6888	**0.0017**	0.05 %/V
PCCi2_FEAST_X_1v8 @ 3.6 A	1.7854	1.7860	1.7869	1.7879	1.7888	1.7900	1.7875	**0.0017**	0.05 %/V
PCCi2_FEAST_Z_1v8 @ 3.6 A	1.8331	1.8343	1.8354	1.8363	1.8377	1.8385	1.8359	**0.0020**	0.06 %/V
PCCi3_bPOL_X_1v8 @ 3.6 A	1.7933	1.7939	1.7942	1.7944	1.7948	1.7954	1.7943	**0.0007**	0.02 %/V
PCCi3_bPOL_Z_1v8 @ 3.6 A	1.8544	1.8550	1.8555	1.8560	1.8571	1.8574	1.8559	**0.0012**	0.03 %/V
PCCi4_bPOL_X_1v8 @ 3.6 A	1.8025	1.8006	1.8010	1.8014	1.8022	1.8026	1.8017	**0.0008**	0.02 %/V
PCCi4_bPOL_Z_1v8 @ 3.6 A	1.8677	1.8679	1.8683	1.8692	1.8698	1.8708	1.8690	**0.0012**	0.03 %/V
PCCi5_bPOL_X_1v8 @ 3.6 A	1.8264	1.8268	1.8274	1.8284	1.8289	1.8297	1.8279	**0.0013**	0.04 %/V
PCCi5_bPOL_Z_1v8 @ 3.6 A	1.8244	1.8248	1.8256	1.8266	1.8269	1.8278	1.8260	**0.0013**	0.04 %/V
PCCi1_FEAST_Y_1v2 @ 1.2 A	1.2062	1.2066	1.2072	1.2078	1.2084	1.2093	1.2076	**0.0012**	0.05 %/V
PCCi2_FEAST_Y_1v2 @ 1.2 A	1.2493	1.2496	1.2505	1.2511	1.2517	1.2522	1.2507	**0.0012**	0.05 %/V
PCCi3_bPOL_Y_1v2 @ 1.2 A	1.2809	1.2813	1.2817	1.2821	1.2827	1.2835	1.2820	**0.0010**	0.04 %/V
PCCi4_bPOL_Y_1v2 @ 1.2 A	1.2895	1.2900	1.2903	1.2908	1.2917	1.2921	1.2907	**0.0010**	0.04 %/V
PCCi5_bPOL_Y_1v2 @ 1.2 A	1.2895	1.2897	1.2903	1.2908	1.2914	1.2918	1.2906	**0.0009**	0.04 %/V
PCCi1_FEAST_W_2v5 @ 0.4 A	2.5433	2.5448	2.5457	2.5465	2.5477	2.5483	2.5461	**0.0019**	0.04 %/V
PCCi2_FEAST_W_2v5 @ 0.4 A	2.6260	2.6272	2.6286	2.6293	2.6307	2.6309	2.6288	**0.0019**	0.04 %/V
PCCi3_bPOL_W_2v5 @ 0.4 A	2.6937	2.6947	2.6958	2.6969	2.6983	2.6994	2.6965	**0.0022**	0.04 %/V
PCCi4_bPOL_W_2v5 @ 0.4 A	2.7043	2.7053	2.7068	2.7076	2.7098	2.7103	2.7074	**0.0024**	0.04 %/V
PCCi5_bPOL_W_2v5 @ 0.4 A	2.7091	2.7103	2.7109	2.7119	2.7133	2.7144	2.7117	**0.0020**	0.04 %/V

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Measurements – Load regulation
(filters and interconnects included)

Table: Measured output voltage evolution for DC-DC converters placed on PCC cards under input voltage conditions expected at full load in CMS BTL project. Load regulation (last column) calculated based on presented measurements.

load current / converter	0.4 A	1.2 A	2.0 A	2.8 A	3.6 A	MEAN	SD	$\Delta V_o/V_o/\Delta I_o$
PCCi1_FEAST_X_1v8 @ 10 V_{in}	1.9028	1.8827	1.8636	1.8467	1.8305	1.8653	0.0286	**-1.21 %/A**
PCCi1_FEAST_Z_1v8 @ 10 V_{in}	1.7628	1.7427	1.7242	1.7065	1.6891	1.7251	0.0290	**-1.34 %/A**
PCCi2_FEAST_X_1v8 @ 10 V_{in}	1.8631	1.843	1.823	1.8055	1.7879	1.8245	0.0297	**-1.29 %/A**
PCCi2_FEAST_Z_1v8 @ 10 V_{in}	1.9087	1.8893	1.8701	1.8531	1.8363	1.8715	0.0286	**-1.21 %/A**
PCCi3_bPOL_X_1v8 @ 10 V_{in}	1.8787	1.8577	1.8372	1.816	1.7944	1.8368	0.0333	**-1.43 %/A**
PCCi3_bPOL_Z_1v8 @ 10 V_{in}	1.9372	1.9171	1.897	1.8764	1.856	1.8967	0.0321	**-1.34 %/A**
PCCi4_bPOL_X_1v8 @ 10 V_{in}	1.8839	1.8636	1.8434	1.8226	1.8014	1.8430	0.0326	**-1.40 %/A**
PCCi4_bPOL_Z_1v8 @ 10 V_{in}	1.9476	1.9279	1.9085	1.8889	1.8692	1.9084	0.0310	**-1.28 %/A**
PCCi5_bPOL_X_1v8 @ 10 V_{in}	1.9077	1.8882	1.8684	1.8484	1.8284	1.8682	0.0314	**-1.33 %/A**
PCCi5_bPOL_Z_1v8 @ 10 V_{in}	1.9035	1.8845	1.8651	1.8455	1.8266	1.8650	0.0305	**-1.29 %/A**
PCCi1_FEAST_Y_1v2 @ 10 V_{in}	1.2299	1.2078	1.1859	1.1658	1.1457	1.1870	0.0333	**-2.22 %/A**
PCCi2_FEAST_Y_1v2 @ 10 V_{in}	1.2725	1.2511	1.2295	1.209	1.1889	1.2302	0.0331	**-2.12 %/A**
PCCi3_bPOL_Y_1v2 @ 10 V_{in}	1.3043	1.2821	1.26	1.2375	1.2148	1.2597	0.0354	**-2.22 %/A**
PCCi4_bPOL_Y_1v2 @ 10 V_{in}	1.3122	1.2908	1.2691	1.2474	1.2255	1.2690	0.0343	**-2.14 %/A**
PCCi5_bPOL_Y_1v2 @ 10 V_{in}	1.3125	1.2908	1.2691	1.247	1.2247	1.2688	0.0347	**-2.16 %/A**
PCCi1_FEAST_W_2v5 @ 10 V_{in}	2.5465	2.5203	2.4967	2.4752	2.4547	2.4987	0.0362	**-1.15 %/A**
PCCi2_FEAST_W_2v5 @ 10 V_{in}	2.6293	2.6029	2.5783	2.5553	2.5334	2.5798	0.0379	**-1.16 %/A**
PCCi3_bPOL_W_2v5 @ 10 V_{in}	2.6969	2.6684	2.6388	2.6091	2.579	2.6384	0.0467	**-1.40 %/A**
PCCi4_bPOL_W_2v5 @ 10 V_{in}	2.7076	2.6819	2.6553	2.6285	2.6014	2.6549	0.0420	**-1.25 %/A**
PCCi5_bPOL_W_2v5 @ 10 V_{in}	2.7119	2.6853	2.6577	2.629	2.6	2.6568	0.0443	**-1.32 %/A**

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Voltage drift estimations for FEASTv2.3

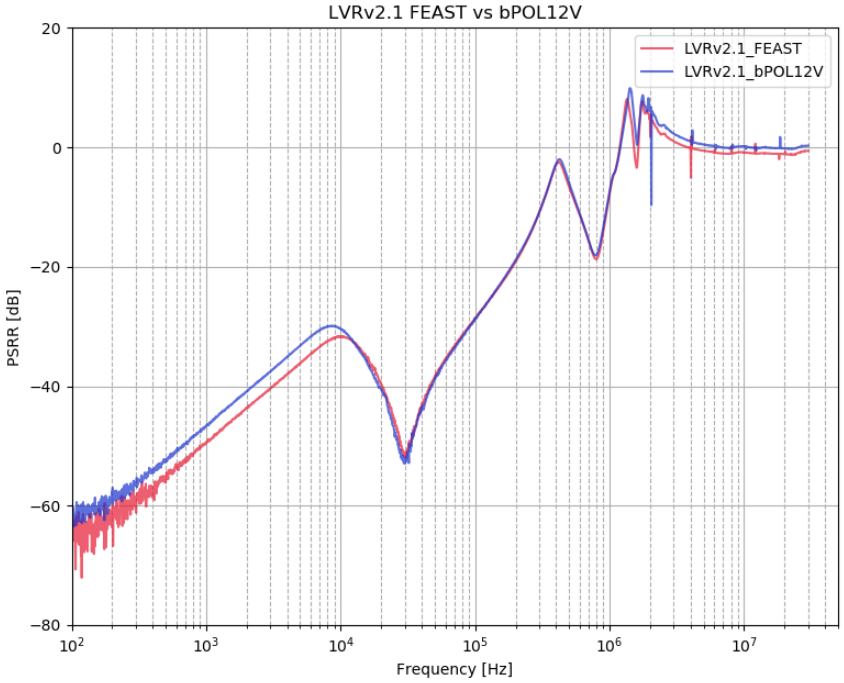
Table: Estimated voltage variations at load for EBUP 1.2 V @ 2A supplied by FEASTv2.3

Source of variation	(MIN – μ)/μ	(MAX – μ)/ μ
Internal reference voltage production spread FEAST	-2.67%	+2.34%
Feedback voltage precision (resistors production spread)	-0.995%	+1.005%
Radiation induced voltage drift at +25°C (0 to 5 Mrad)	+0.40%	+0.40%
V_{ref} drift with temperature for FEASTv2.3 From (room temperature to + 60°C, ΔT_{MAX} = 40°C)	+0.84% [+0.021%/°C]	+0.84% [+0.021%/°C]
PCB temperature impact on the V_o drift for ECAL 1.2 V @ 2.0 A (ΔT_{MAX} = 20°C)	-0.5% [-0.0250%/°C]	-0.5% [-0.0250%/°C]
Load regulation (converter + power distribution network)	**-4.44% [-2.22 %/A]**	**-4.24% [-2.12 %/A]**
SUMMARY:	-7.37%	-0.16%
SUMMARY (day 0 - no radiation):	**-7.77%**	**-0.56%**
Rebalanced for half of TID (V_o shifted by +3.76%)	-3.61%	+3.61%

Table: Estimated voltage variations at load for BTL 1.2 V @ 1.2A supplied by FEASTv2.3

Source of variation	(MIN – μ)/μ	(MAX – μ)/ μ
Internal reference voltage production spread FEAST	-2.67%	+2.34%
Feedback voltage precision (resistors production spread)	-0.995%	+1.005%
Radiation induced voltage drift at -25°C (0 to 5 Mrad)	+1.59%	+1.59%
V_{ref} drift with temperature for FEASTv2.3 From (room temperature to - 35°C, ΔT_{MAX} = -55°C)	-1.16% [+0.021%/°C]	-1.16% [+0.021%/°C]
PCB temperature impact on the V_o drift for ECAL 1.2 V @ 2.0 A (ΔT_{MAX} = 20°C)	-0.5 % [-0.0250%/°C]	-0.5% [-0.0250%/°C]
Load regulation (converter + power distribution network)	**-2.66% [-2.22 %/A]**	**-2.54% [-2.12 %/A]**
SUMMARY:	-6.39%	0.74%
SUMMARY (day 0 - no radiation):	**-7.98%**	**-0.85%**
Rebalanced for half of TID (V_o shifted by +3.62%)	-3.57%	+3.57%

Measurements – Power Supply Rejection Ratio



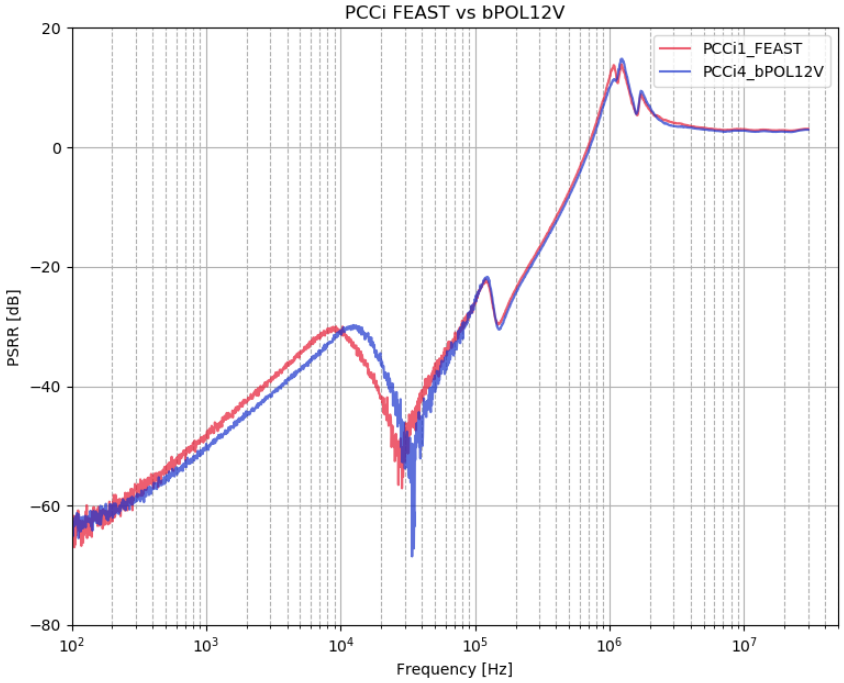


Figure: PSRR plots measured on two types of cards LVR and PCC, carrying both bPOL and FEAST ASIC.

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Observed features - oscillations

- **Normal state of the output voltage of the affected converter:**

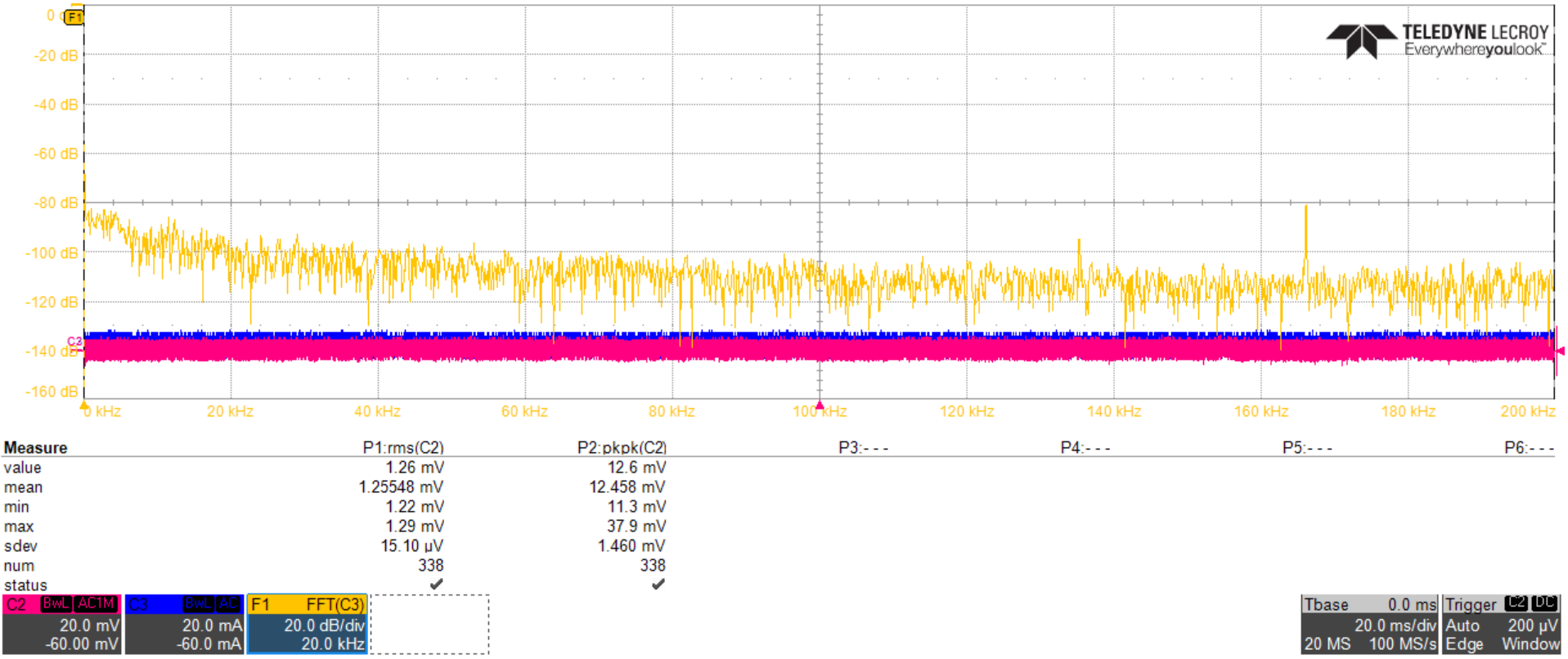
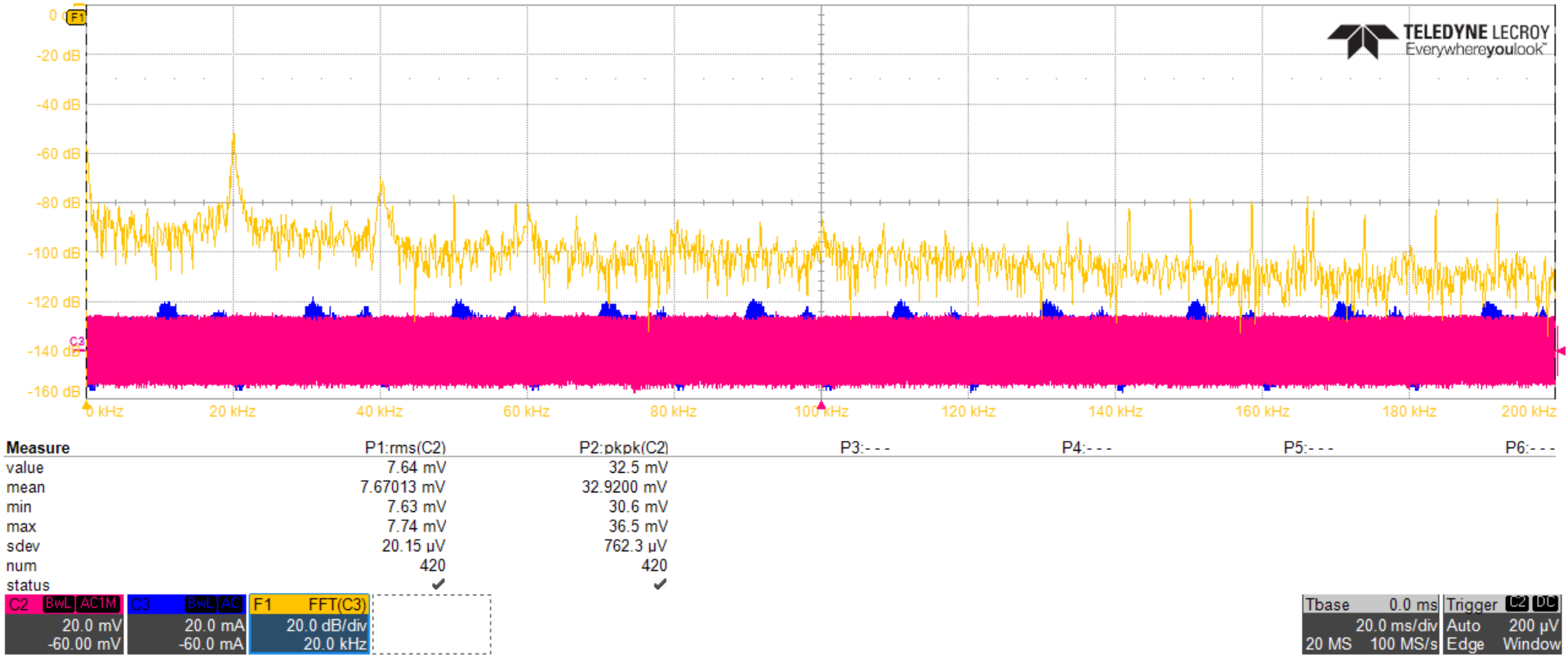


Figure: No oscillation recorded on the PCCi5 card with bPOL regulating 1.8 V; V_{in} = 8 V; A_{out} = 0.0 A.
Pink plot - AC coupled output voltage, Blue plot - AC coupled output current, Yellow plot – FFT of output current

Observed features - oscillations

- **"Oscillatory" state of the affected converter:**



Measure	P1:rms(C2)	P2:pkpk(C2)	P3:- - -	P4:- - -	P5:- - -	P6:- - -
value	7.64 mV	32.5 mV				
mean	7.67013 mV	32.9200 mV				
min	7.63 mV	30.6 mV				
max	7.74 mV	36.5 mV				
sdev	20.15 µV	762.3 µV				
num	420	420				
status	✔	✔				

C2 BwL AC1M	C3 BwL AC	F1 FFT(C3)	Tbase 0.0 ms	Trigger C2 DC
20.0 mV	20.0 mA	20.0 dB/div	20.0 ms/div	Auto 200 µV
-60.00 mV	-60.0 mA	20.0 kHz	20 MS 100 MS/s	Edge Window

Figure: Oscillation recorded on the PCCi5 card with bPOL regulating 1.8 V; V_{in} = 8 V; A_{out} = 0.67 A.
Pink plot - AC coupled output voltage, Blue plot - AC coupled output current, Yellow plot – FFT of output current

Website

http://eth.app.cern.ch/