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Prototyping Serial Powering for the ATLAS ITk Pixel Detector

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The high luminosity upgrade for the LHC at CERN requires a complete overhaul of the current inner detectors of ATLAS and CMS. A serial powering scheme has been chosen to cope with the constraints of the new pixel detectors. A prototype stave consisting of up to 8 quad modules, based on the new readout chips developed by the RD53 collaboration in 65 nm CMOS technology, RD53A and ITkPixV1, has been set up in Bonn. This contribution covers the results obtained with RD53A modules and presents first measurements with a full ITkPixV1.1 serial powering chain.

Summary (500 words)

For the high luminosity upgrade of the LHC, the current tracking detectors of the ATLAS and CMS experiments will be replaced by completely new tracking detectors. To cope with the harsh radiation environment and high hit rates expected in the inner pixel layers, a new readout chip for both detectors is designed by the RD53 collaboration in 65 nm CMOS technology. Compared to previously built pixel detectors, the new readout chip will feature a significantly smaller pixel size and hence a significantly increased current consumption. Considering the limited space that is available for services routing and the need to minimize material and power budget in the detector, serial powering has been chosen as a baseline for both upgrade projects.

In the upgraded ATLAS pixel detectors, a serial powering chain will consist of up to 14 pixel modules, each consisting of up to 4 readout chips connected in parallel. A constant current is supplied to the chain, where the maximum chain current is defined by the maximum current consumption of the front-end chip and an additional headroom to compensate static and dynamic variations of the on-module current distribution. The key components of such serially powered system are the Shunt-Low Dropout regulators (SLDO) integrated in the readout chip. A SLDO converts the constant supply current to a constant supply voltage for the readout chip, any excess current is shunted by the regulator. With two SLDOs integrated on each readout chip, the serial powering chain current is distributed between up to 8 SLDOs. This powering scheme offers a significant reduction in material and power budget compared to the conventional parallel powering scheme, but provides additional challenges for the electrical and mechanical design: the module stability and the stability and monitoring of the chain as a whole, the choice of the high voltage (HV) distribution scheme, the grounding scheme and the cooling of the SLDO regulators have to be considered in particular.
Several prototyping campaigns aim at verifying the different aspects of serial powering. In Bonn, a prototype consisting of up to 8 quad-chip modules, using either RD53A or ITkPixV1.1 readout chips, has been set up. This prototype aims to study low-level system aspects of serial powering. Using fully functional RD53A modules with planar sensors, the behaviour and performance of current generation readout chips in a serially powered system, on-module current distribution and supply current headroom as well as the choice of the sensor high voltage distribution scheme have been studied.
Currently the prototype is loaded with ITkPixV1.1 digital quad modules with no sensor. The immediate aim of this setup is to provide input for the low voltage power supply market survey for the ITk Pixel detector. In the following the studies performed with the RD53A powering chain will be built upon and expanded with ITkPixV1.1 modules.

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