Contribution ID: **20** Type: **Oral**

The ALICE central trigger system for LHC Run 3

Tuesday, 20 September 2022 14:00 (20 minutes)

The LHC interaction rate at ALICE will be increased to 50 kHz in Pb–Pb collisions and 1 MHz in pp collisions. In order to read out data at these interaction rates the ALICE Central Trigger System was upgraded for LHC Run 3 with completely new hardware and a new Trigger and Timing System, based on a Passive Optical Network. The main hardware is a universal trigger board based on the Xilinx Kintex Ultrascale FPGA, which can function as a Central Trigger Processor, Local Trigger Unit and monitoring interfaces. The trigger system, its installation and commissioning will be presented.

Summary (500 words)

In LHC Run 3 the interaction rates in ALICE at LHC Point 2 will increase to 50 kHz for Pb-Pb, and up to 1 MHz for pp and p-A. The aim of the ALICE trigger system is to select essentially all these interactions. Most ALICE detectors feature continuous read-out. Regular "Heartbeat"triggers and "Time frame"triggers are used to delimit data for detectors running in continuous mode. The Central Trigger System (CTS) must also cope with detectors that still have dead-time during readout. The CTS provides minimum bias triggers for commissioning and dedicated runs in triggered mode and for all detectors without continuous readout, at three different latencies (referred to as LM, L0, and L1) depending on the timing requirements of each detector. The CTS consists of "Central Trigger Processor"(CTP) and "Local Trigger Unit"(LTU) modules. Both module type are based on the same HW (trigger board), but have different FPGA and FMC card. The LTU has the Xilinx Kintex Ultrascale FPGA XCKU040FFVA1156-2E and the CTP has a XCKU060FFVA1156-2E. The trigger board has several interfaces: upgraded Timing, Trigger and Control Passive Optical Network (TTC-PON), GBT, IPbus, I2C, SPI and the original TTC. The board is equipped with 2 DDR4 memories (each 1 GB) and can be equipped with a maximum of 20 SFP+ modules. A complex power system on the board is controlled by two UCD90120A power sequencers and is monitored via Power Management bus. The main interface between the LTU and the "Common Readout Unit"(CRU) will be TTC-PON, but the latency critical detectors will also receive triggers directly at their FEE via GBT (in parallel to CRU via TTC-PON) due to trigger latency constraints. The interface between the CTP and the LTU is also based on TTC-PON, but for latency critical detectors there is the option to deliver the trigger signal via a copper cable. The LTU collects all BUSY signals from the detectors and forward these to the CTP (TTC-PON time multiplexed upstream) where an overall BUSY mask is built. The CTS is connected to the ALICE readout via its own dedicated CRU, such that trigger decisions are recorded together with the detector data. In addition, the system monitors the status of all CRUs and is able to throttle the readout rate depending on the CRU buffers status.
The final VME boards were produced and tested in summer 2020, and the boards were installed in the ALICE cavern (LHC Point 2). In autumn 2021, the full setup, consisting of the CTP and 16 LTUs was tested during the LHC Pilot Test Beam. Five types of firmware and software have been developed for these CTS components: the CTP, the LTU (2 fiirmware versions), Trigger and Timing Control interface test, Trigger Input and Clock Generator and 4 types of firmware and software for the board test. All types of firmware and software are thoroughly tested on a test setup in the CTP lab before installation in the ALICE experiment.

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Session Classification: Trigger

Track Classification: Trigger