Contribution ID: **123** Type: **Oral**

Architecture and Prototype of the CMS Global Level-1 Trigger for Phase-2

Tuesday, 20 September 2022 11:20 (20 minutes)

We present the architecture and current state of prototype firmware of the CMS Level-1 Global Trigger, the final stage of the Level-1 trigger for Phase-2 of the operation of the LHC. Based on high-precision inputs from the muon-, calorimeter-, track- and particle flow triggers, the Global Trigger evaluates O(1000) cut-based and neural-net based algorithms in a system of up to thirteen Xilinx Ultrascale Plus based ATCA processing boards interconnected by 25 Gb/s optical links. In order to optimize usage of resources and to facilitate routing, the main algorithms, including the DSP-based calculation of invariant masses, are implemented at 480 MHz.

Summary (500 words)

For Phase-2 of the operation of the LHC, starting in 2029, CMS will undergo major upgrades to its detectors and readout electronics. A completely new first-level trigger system will ensure that the excellent physics performance of CMS is maintained or improved under the challenging pile-up conditions in Phase-2. The new trigger system, based on generic ATCA processing boards hosting Xilinx Ultrascale Plus FPGAs and interconnected with links at 25 Gb/s, will exploit high granularity information from the calorimeters, muon systems and a track finder, reconstructing tracks from the silicon strip tracker at the bunch crossing rate. The trigger system will contain algorithms such as particle flow that previously only have been employed in software at the higher trigger levels. The final stage in the level-1 trigger, the Global Trigger (GT), will receive high-precision trigger objects from the muon-, calorimeter-, track- and particle flow triggers. It will evaluate a menu of O(1000) cut-based and neural-net based trigger algorithms in order to determine the level-1 trigger accept decision. Cut-based algorithms may include conditions on event topology such as the angle between particles or the invariant mass of a hypothetical mother particle of two decay products. While most upstream systems of the GT are implemented in a time-multiplexed way, the GT itself works in in a non-time-multiplexed fashion in order to enable the search for certain long-lived particles that require the correlation of objects in neighboring bunch crossings. Up to twelve generic processing boards will each receive a copy of all inputs from the upstream systems, so that algorithms can be freely assigned to any processing board. A 13th generic processing board, the Final-OR board, is planned to handle pre-scaling and monitoring of the algorithms, assignment of the trigger type, merging of the trigger decision and its transmission to the Trigger Control and Distribution system. The target board for all thirteen processing boards in the GT is the Serenity board built by Imperial College, equipped with a single VU13P FPGA.
Prototype firmware has been developed for a pre-production prototype of the Serenity board with a VU9P FPGA. This algorithm firmware includes the de-multiplexing logic handling data from time-multiplexed upstream systems, conversion to an internal common object format, distribution of trigger objects across the Super Logic Regions of the FPGA and a simplified menu composed of di-object conditions with and without topological conditions. In order to use resources efficiently and to facilitate routing of the FPGA, the cut-based algorithms, including algorithms that use DSPs to calculate topological relations between objects, have been implemented at 480 MHz. Prototype firmware covering 66 out of 78 planned upstream links and handling 234 simultaneous trigger algorithms, 30% of which utilize DSP-based calculations, has been successfully implemented and verified to be bit-wise compatible with a C++ based simulation of the algorithms. The firmware meets the latency requirements set out in the corresponding Technical Design Report. First tests in hardware

have been performed with a prototype of an upstream system.

Primary author: SAKULIN, Hannes (CERN)

Co-authors: HUBER, Benjamin (Technische Universitaet Wien (AT)); RABADY, Dinyar (CERN); LEUTGEB, Elias (Technische Universitaet Wien (AT)); BORTOLATO, Gabriele (Universita e INFN, Padova (IT))

Presenter: SAKULIN, Hannes (CERN)

Session Classification: Trigger

Track Classification: Trigger