

Sector Logic Development for the ATLAS Level-0 Muon Trigger at HL-LHC

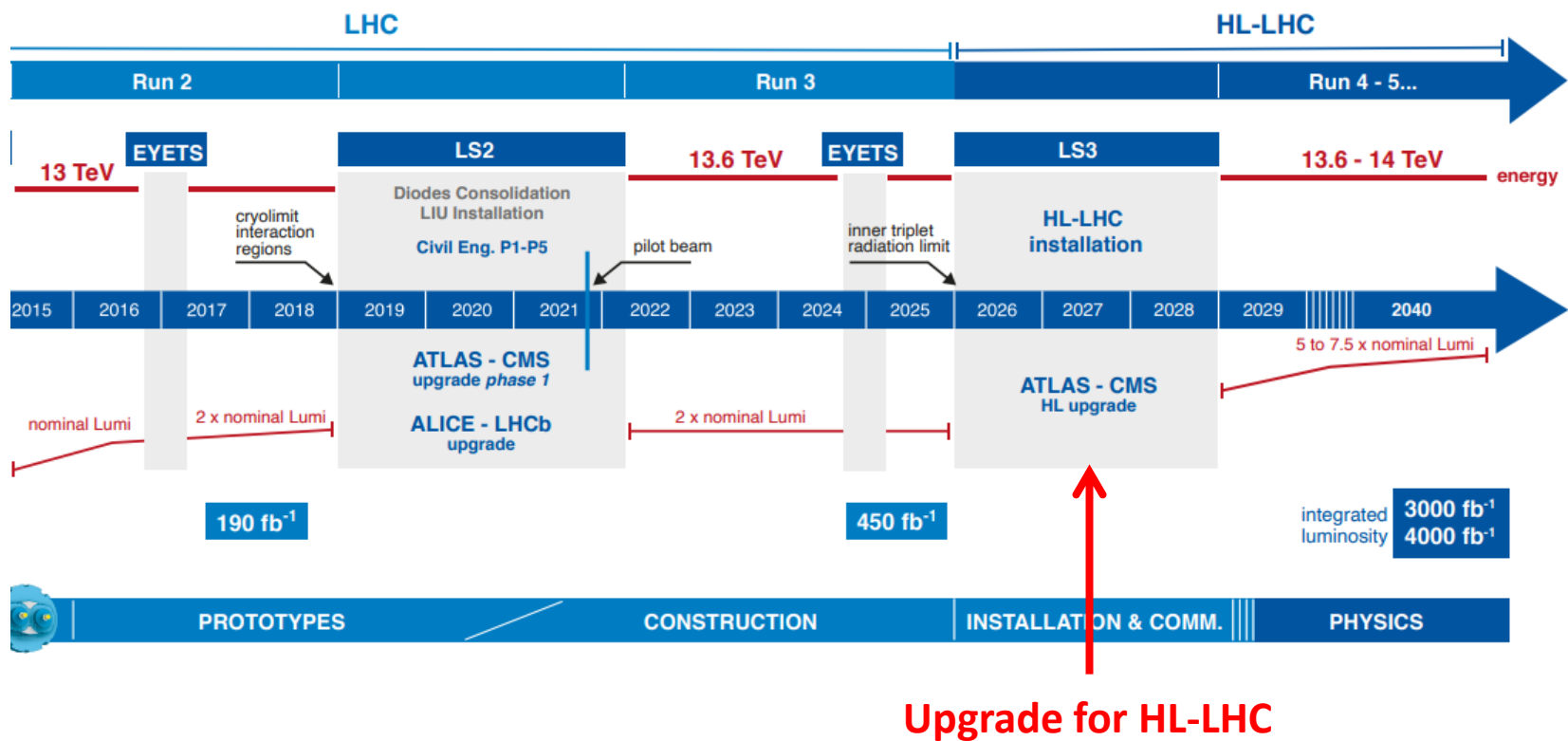
TWEPP 2022 @Bergen, Norway
September 20th, 2022

Yuki Mitsumori (Nagoya University)
on behalf of the ATLAS Collaboration



Introduction

High-Luminosity LHC (HL-LHC) is planned to start its operation in 2029 to deliver larger amount of collision data.



ATLAS Trigger and DAQ Upgrade for HL-LHC

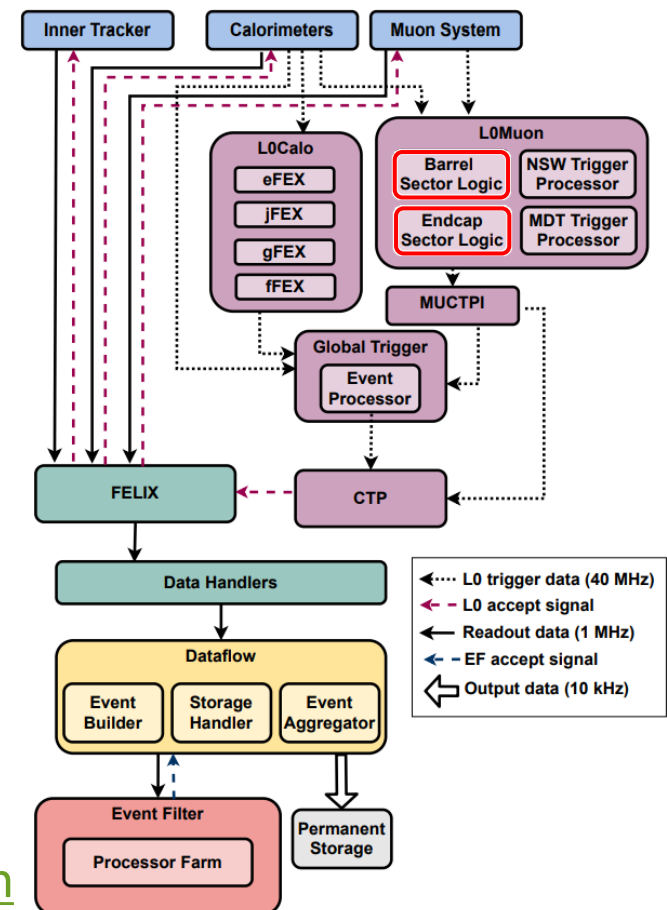
The current trigger and DAQ system will be upgraded toward HL-LHC.

- Level-1 (L1) trigger used for LHC will be replaced by Level-0 (L0) trigger.

	LHC	HL-LHC
L1/L0 trigger rate [MHz]	0.1	1
L1/L0 trigger latency [μs]	2.5	10

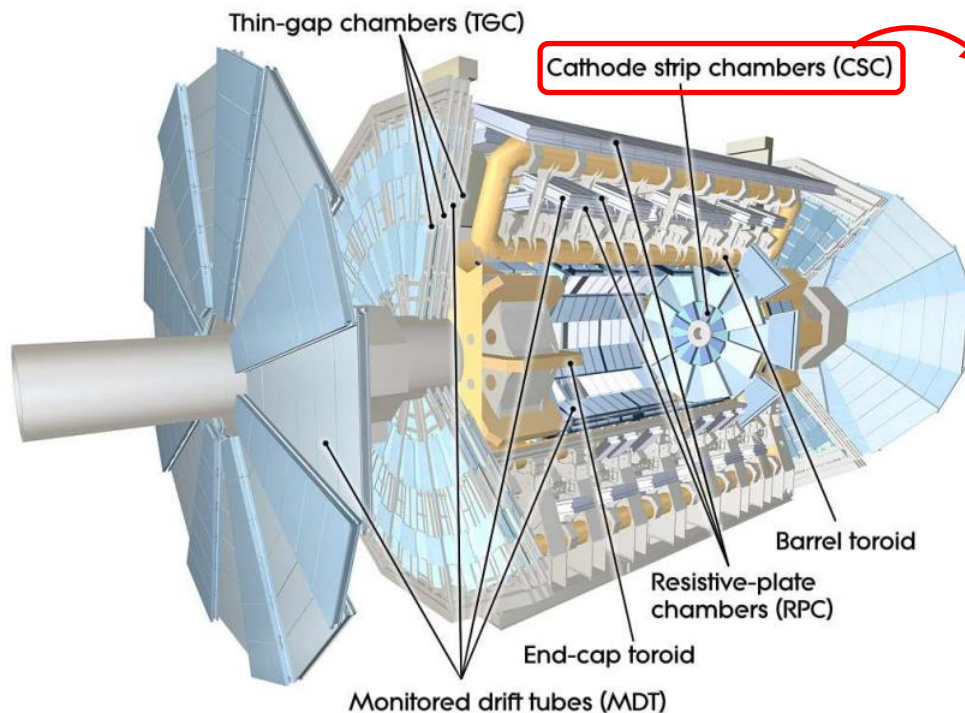
Three presentations for L0 muon trigger

- Barrel/Endcap Sector Logic: **this talk**
- RPC electronics including Barrel Sector Logic: [poster by F. Morodei](#)
- MDT Trigger Processor: [talk by P. Sundararajan](#)

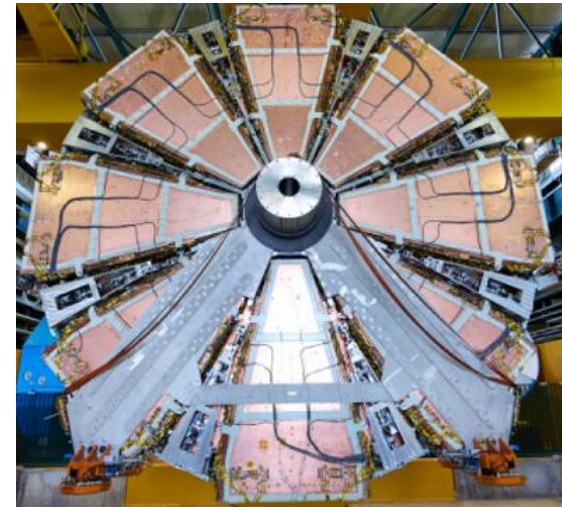


ATLAS Muon Spectrometer

ATLAS muon spectrometer consists of various sub-detectors.



Replaced by **New Small Wheel (NSW)**



- Micro-mesh gaseous detectors
- small strip TGCs

Overview of the L0 Muon Trigger

1. Reconstruct muon candidates from TGC/RPC hits
2. Select muon candidates with higher transverse momenta (p_T) than trigger threshold by using various detector signals

Resistive Plate Chamber (RPC)

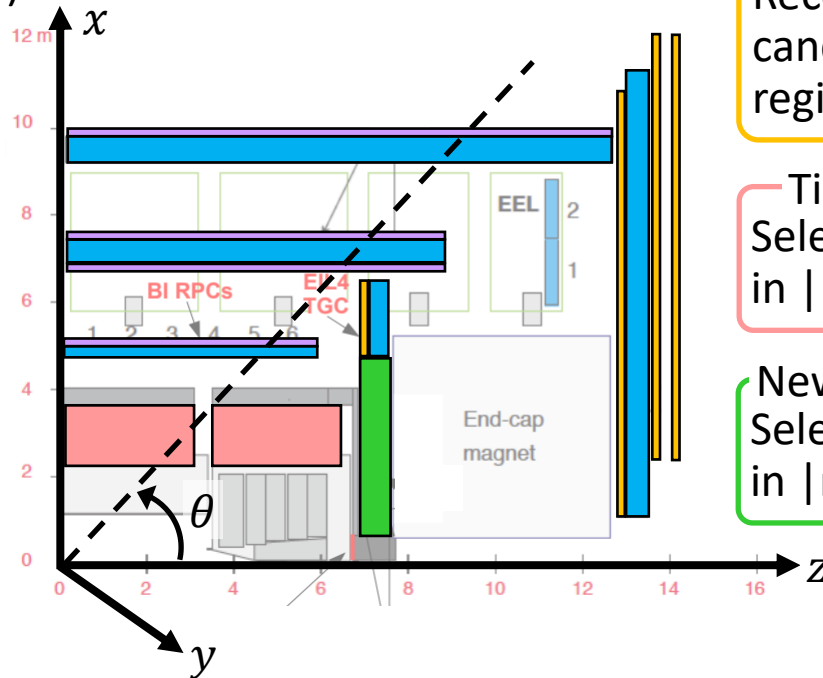
Reconstruct muon candidate in the barrel region ($|\eta| < 1.05$)

Monitored Drift Tube (MDT)

Select muon candidate in the barrel and endcap

$$\text{Pseudorapidity } \eta = -\ln \tan\left(\frac{\theta}{2}\right)$$

$$\text{Azimuthal angle } \phi = \tan^{-1}\left(\frac{y}{x}\right)$$



Thin Gap Chamber (TGC)
Reconstruct muon candidate in the endcap region ($|\eta| = 1.05 - 2.4$)

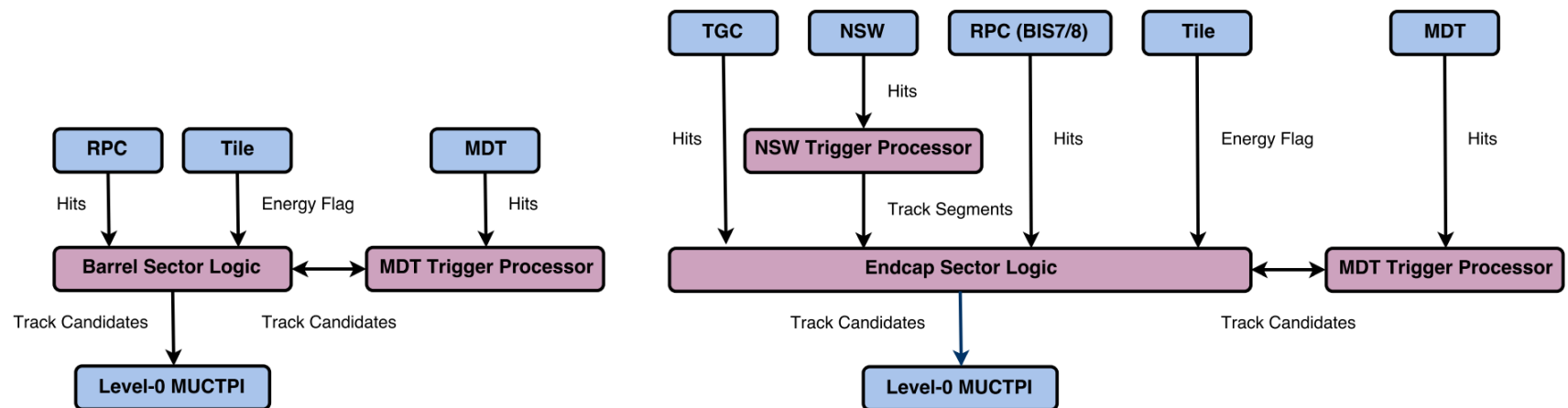
Tile calorimeter (Tile)
Select muon candidate in $|\eta| < 1.3$

New Small Wheel (NSW)
Select muon candidate in $|\eta| = 1.3 - 2.4$

Sector Logic (SL)

Sector Logic (SL) boards have three functions:

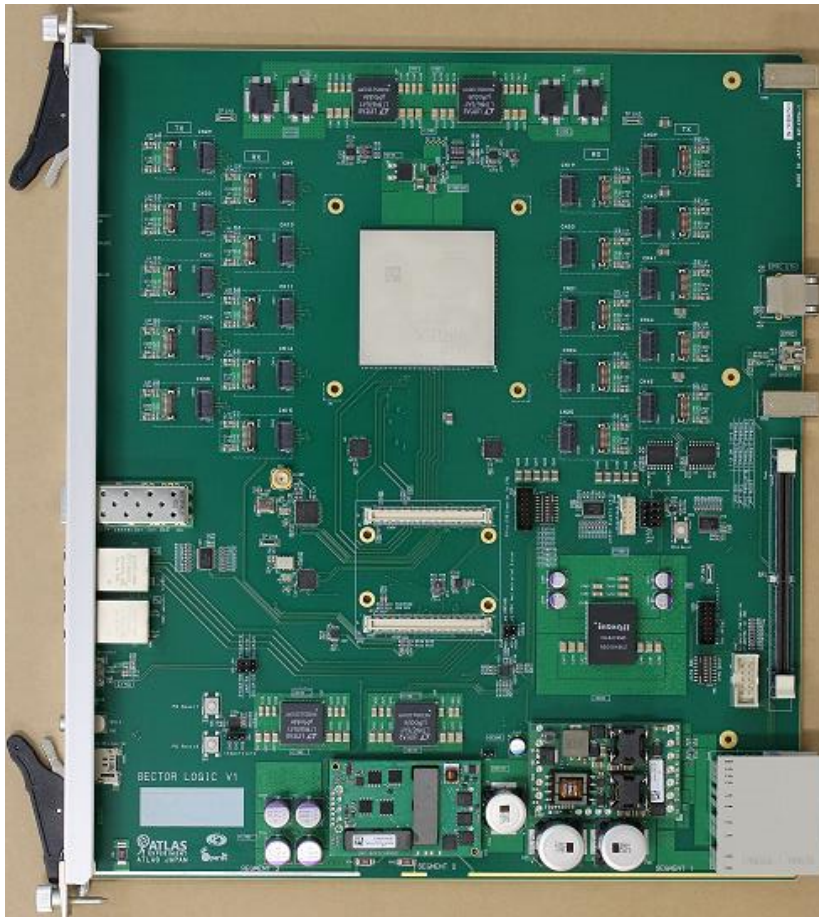
- Reconstruct and select muon candidates for the L0 muon trigger using the data from several detectors (see previous page)
- Readout the hit data of RPC/TGC at the barrel/endcap
- Control and monitor RPC/TGC frontend boards at the barrel/endcap



Barrel and endcap SL boards have a common hardware design.

Overview of SL Board

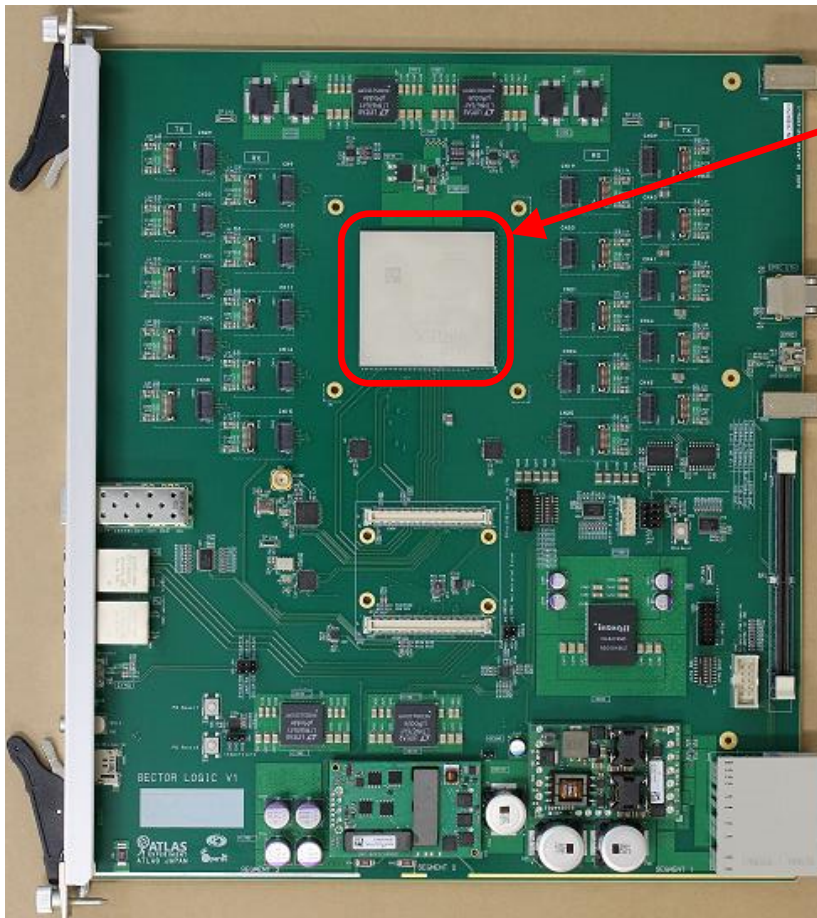
First prototype of the SL board produced in Oct. 2021



Form factor: ATCA

Overview of SL Board

First prototype of the SL board produced in Oct. 2021

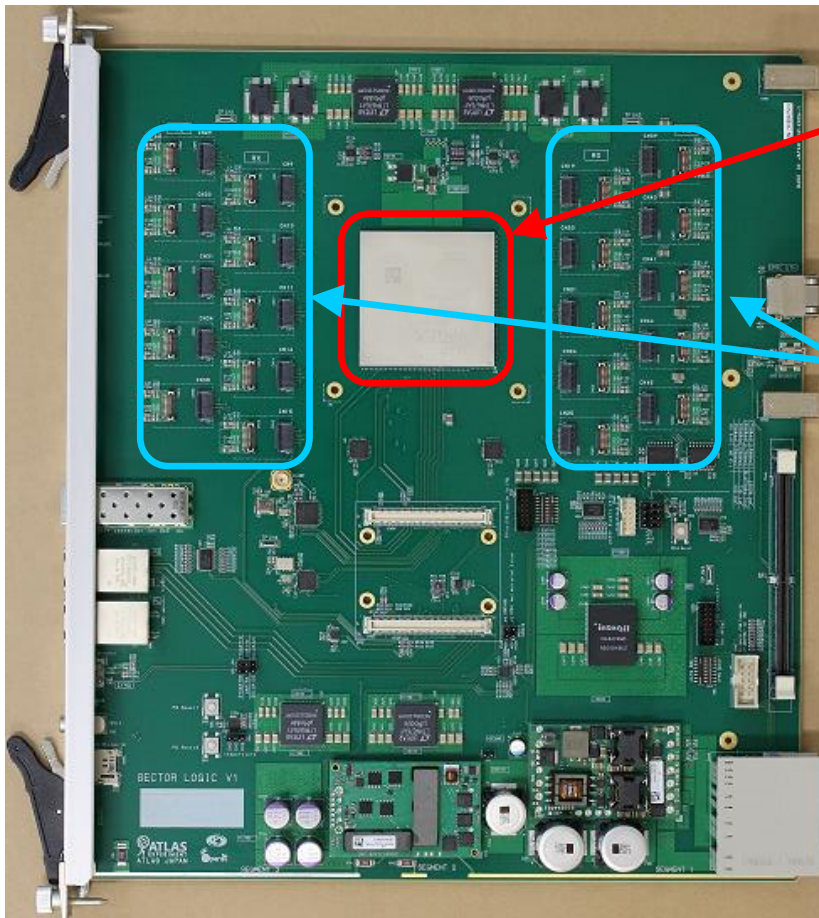


- Large-scale FPGA
 - Xilinx XCVU13P
 - Trigger and readout functions
 - Control/monitor on-detector boards

Form factor: ATCA

Overview of SL Board

First prototype of the SL board produced in Oct. 2021



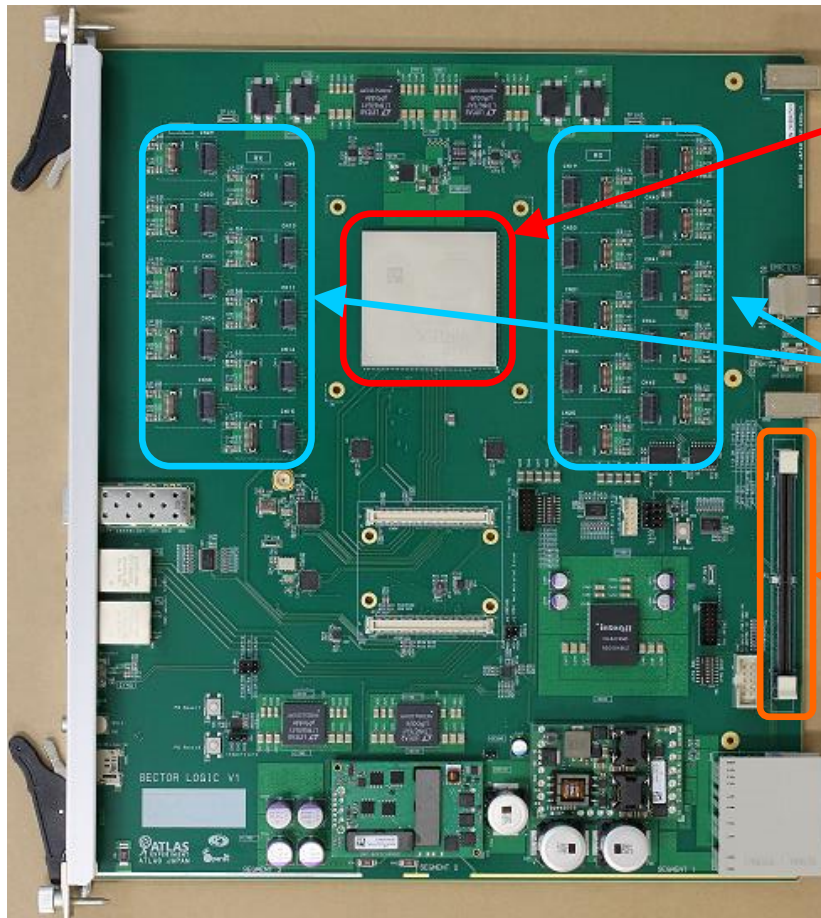
- Large-scale FPGA
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- Optical transceiver
 - 120 pairs of TX and RX lanes of FireFly
 - Receive detector signals and transmit trigger and readout outputs

Form factor: ATCA

Overview of SL Board

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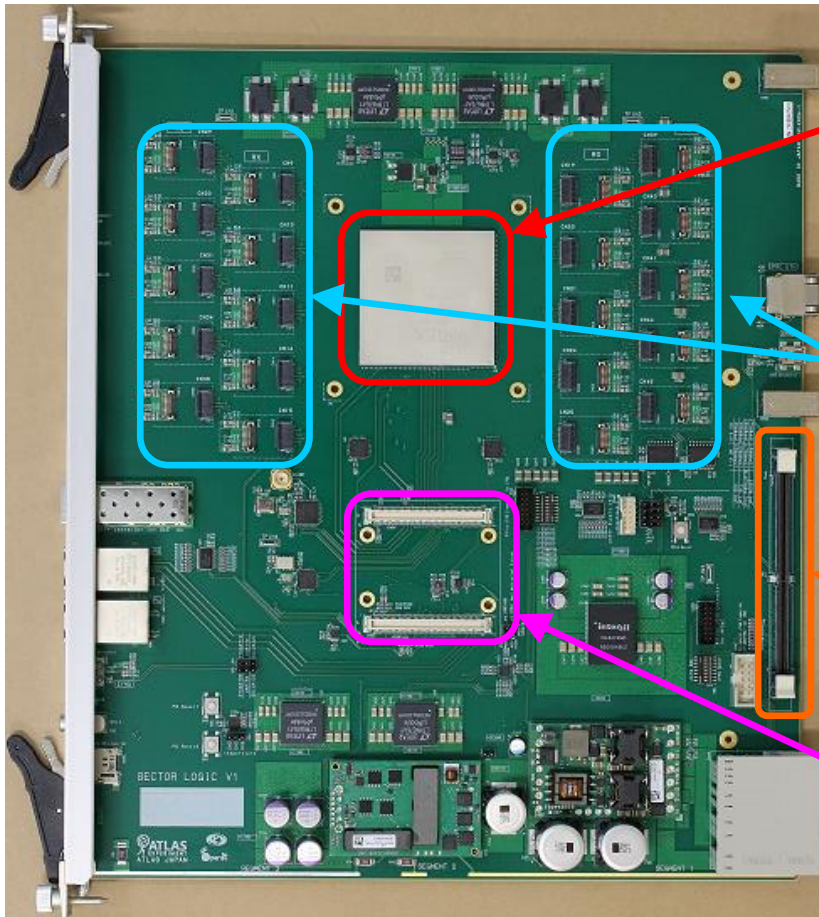
- Optical transceiver
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- IPMC mezzanine card
 - CERN-developed IPMC
 - Control/monitor power supply

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- MPSoC mezzanine card
 - Enclustra Mercury XU5
 - Control/monitor the FPGA

Form factor: ATCA

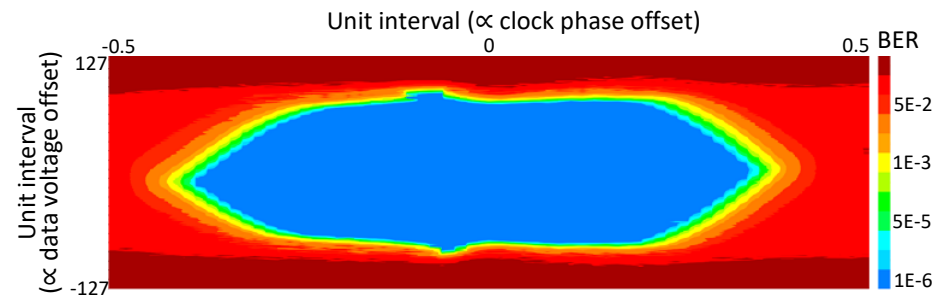
Test of the First SL Prototype

Most of the tests completed

- Power up/down sequencing
- Temperature monitoring
- FPGA configuration and initial trigger firmware test
- FireFly loopback
- MPSoC-FPGA connection
- IMPC-Shelf manager connection
- Clock recovery for fixed latency (zero delay mode of Si5345)

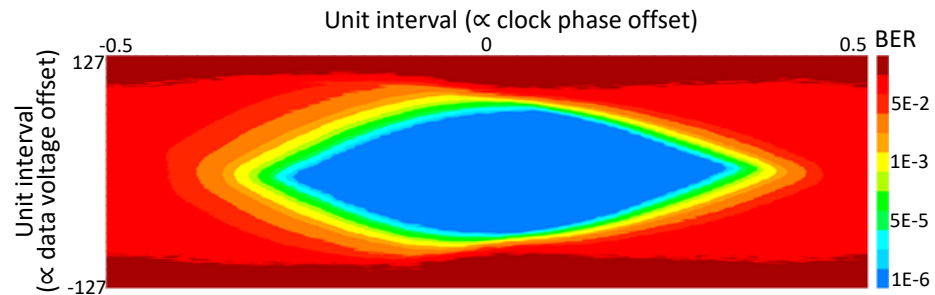
Result of FireFly loopback test with [Xilinx IBERT](#)

9.6 Gb/s assumed max rate for SL



Nominal point (dedicated measurement):
BER < 3.4×10^{-15} (95 % C.L.)

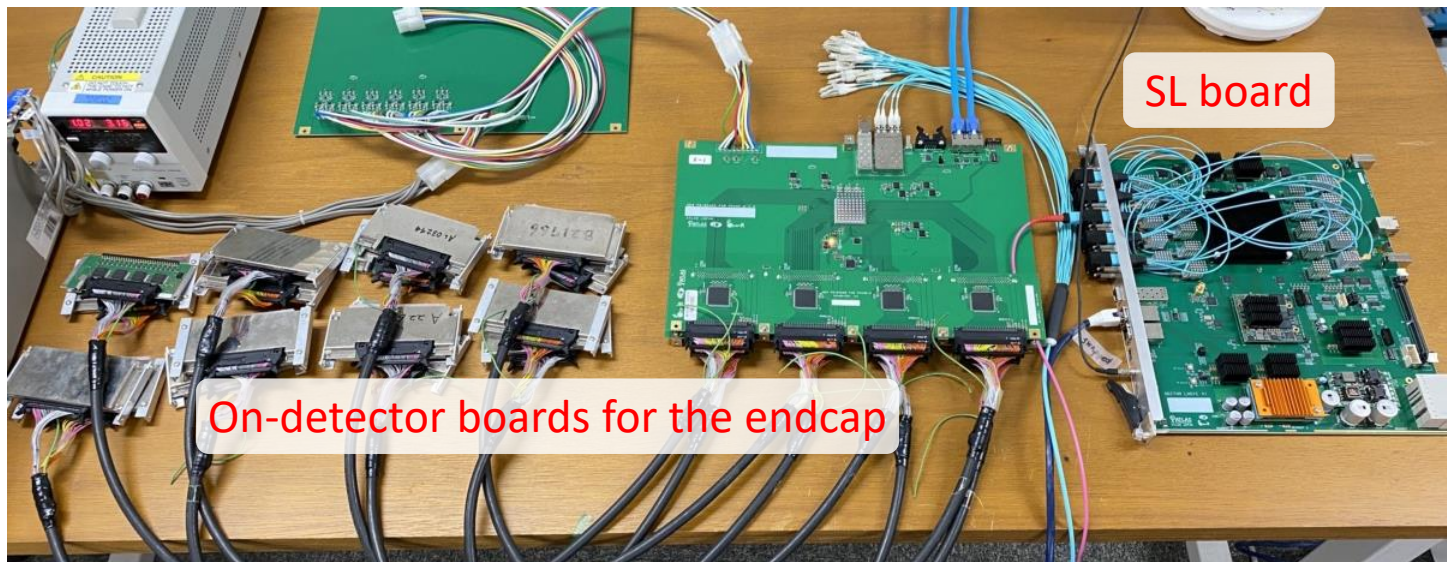
18.0 Gb/s as a test of board capacity



$$\text{BER (Bit Error Ratio)} = \frac{\text{Number of error bits}}{\text{Number of transferred bits}}$$

System-Level Commissioning

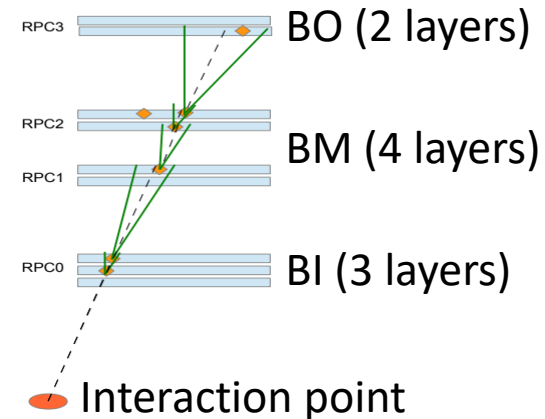
- Control registers on each peripheral and on FPGA from MPSoC
- Readout path established for the endcap system
- Trigger firmware tests ongoing



[Talk by T. Aoki](#)

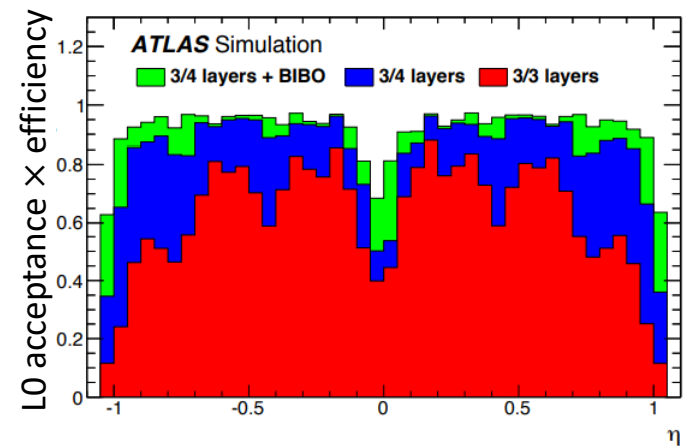
Barrel Trigger Logic

- RPC hits are linked between consecutive planes based on pre-defined coincidence windows centered on a straight-line extrapolation from the nominal interaction point.



- Acceptance \times efficiency will be improved by installing additional RPC chambers in the barrel inner station (BI).

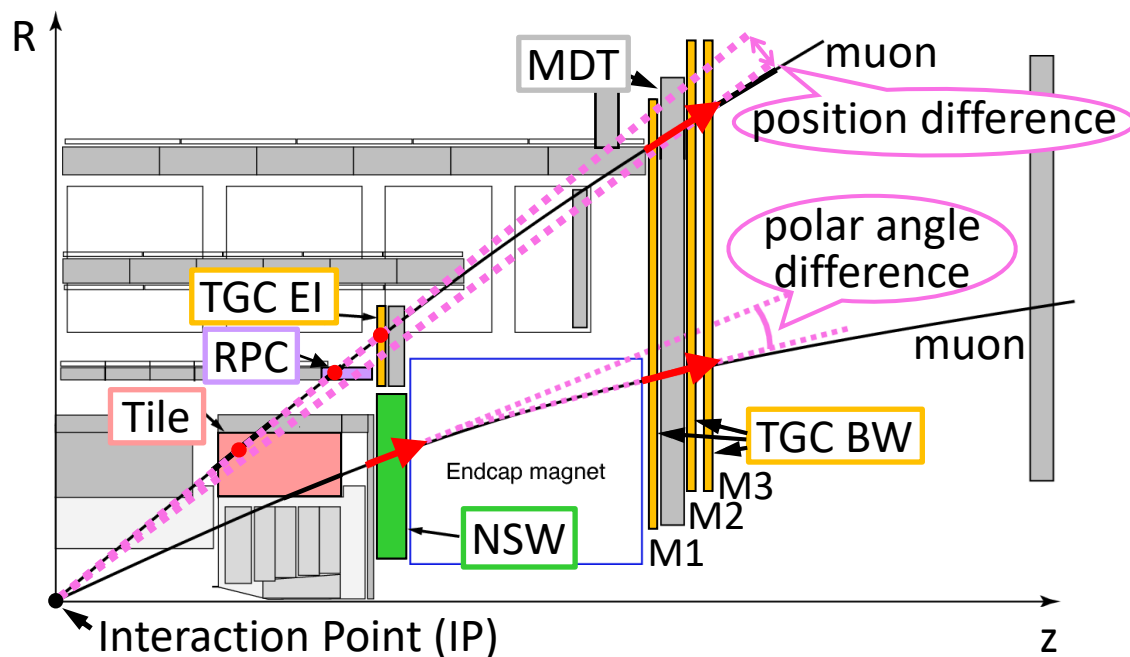
→ Firmware development is ongoing.



L0 acceptance \times efficiency obtained with respect to offline reconstructed muons

Endcap Trigger Logic

- Muon candidates are reconstructed with hits of TGC Big Wheel (BW). (“TGC track segment reconstruction”, see next page)
- Muon candidates are selected with the data from other detectors based on information before and after magnetic field.



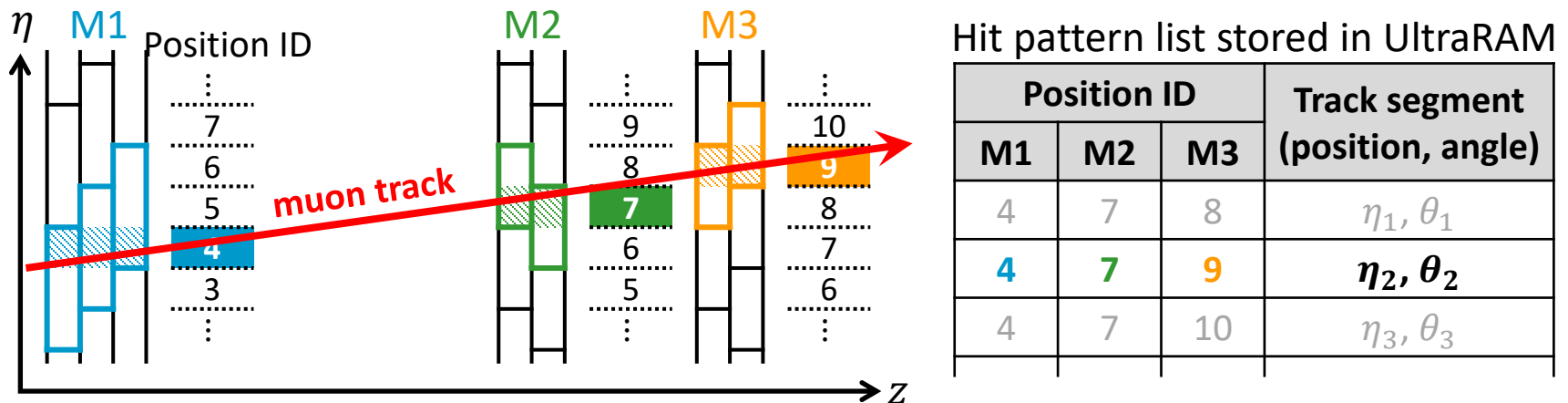
Position difference (η, ϕ):
between track segment
reconstructed from TGC BW
and hits from TGC EI, RPC
and Tile

Polar angle difference:
between track segment
reconstructed from TGC BW
and that from NSW.

TGC Track Segment Reconstruction (1)

Track segments reconstructed by “pattern-matching” algorithm

- ① Take coincidence and output position IDs in each of three stations: **M1** (3 layers), **M2** (2 layers) and **M3** (2 layers)
- ② Combine position IDs on three stations and obtain segment data from FPGA UltraRAM where segment data are stored



TGC Track Segment Reconstruction (2)

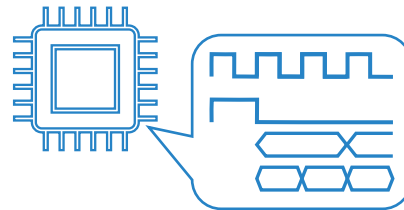
The TGC track segment reconstruction firmware implemented and validated in firmware simulation

TGC hits from
ATLAS Geant4 simulation



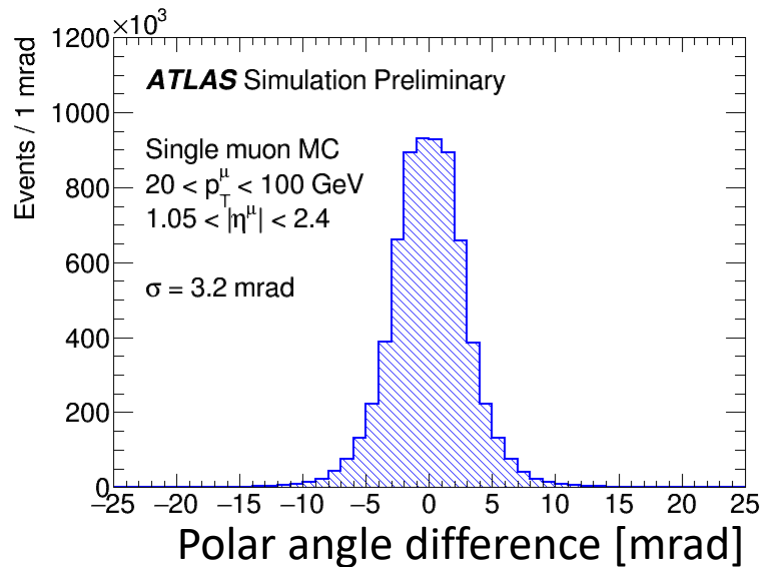
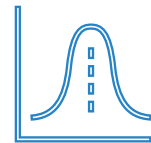
40.079 MHz

Vivado RTL simulation



Waveform output

Performance
evaluation

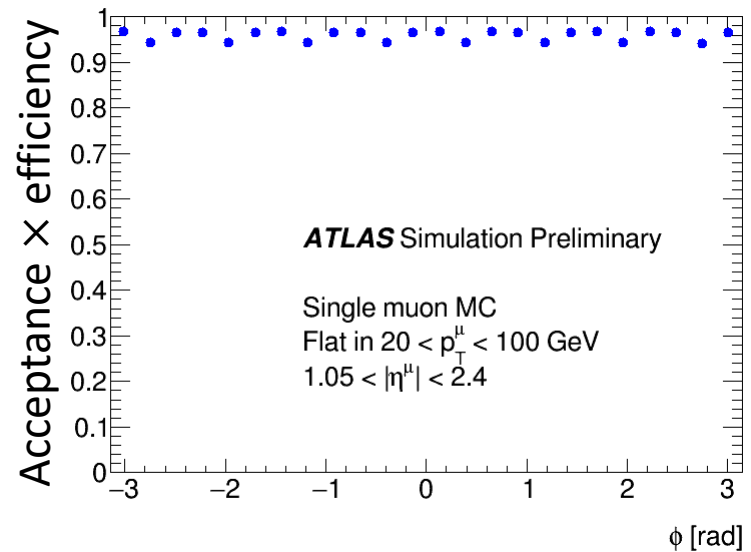
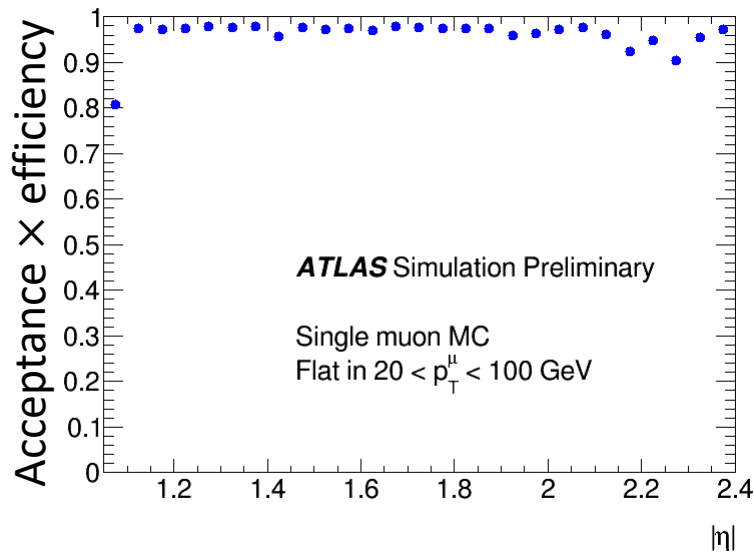


Good results obtained

- Angular resolution: **3.2 mrad**
- Reconstruction efficiency: **96 %**

TGC Track Segment Reconstruction (3)

A high efficiency obtained for whole endcap region



Smaller efficiencies in several bins ($|\eta| \sim 1.4$ and 2.2 , one out of three ϕ bins) due to TGC detector holes for the laser paths of the MDT alignment system

Conclusions

- ATLAS Trigger and DAQ systems will be upgraded for HL-LHC.
- Sector Logic is a core part of the new L0 muon trigger. Barrel/Endcap Sector Logic are based on the same hardware design.
- First hardware prototype of the SL board was produced and almost all tests were completed successfully.
- In the barrel region, additional RPC detectors in the inner station will increase trigger acceptance.
- In the endcap region, new logic using various detectors will improve selectivity.
- TGC track segment reconstruction firmware has been implemented for the full coverage of the detector and good efficiencies and angular resolutions have been obtained.