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Sector Logic Development for the ATLAS Level-0 Muon Trigger at HL-LHC

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The design of the Sector Logic (SL) for the ATLAS Level-0 muon trigger at HL-LHC and the milestones achieved on the hardware and firmware developments are presented. The first prototype of the SL board was produced, and all the functions have been demonstrated and confirmed. Fast tracking using Thin Gap Chamber (TGC) hits, a core part of the Level-0 muon trigger, has been developed for full coverage of the endcaps and the performance was confirmed with post-synthesis simulations, demonstrating the feasibility of processing the TGC hits from ˜7000 channels within ˜100 ns using single XCVU13P FPGA for muon tracking.

Summary (500 words)

HL-LHC will start operations in 2029 to deliver more than ten times the integrated luminosity of the LHC Runs 1-3. In order to cope with the proton-proton collision rate higher than that of LHC, the trigger and readout system of the ATLAS experiment needs to be replaced. The new Level-0 muon trigger system is required to reconstruct muon candidates with an improved momentum resolution to suppress the trigger rate with keeping the efficiency. That can be achieved by combining the signals from various subdetectors: Resistive Plate Chamber (RPC), Thin Gap Chamber (TGC), New Small Wheel (NSW), Monitored Drift Tube (MDT), and scintillator-steel hadronic calorimeters (TileCal) to form more offline-like tracks.

The Sector Logic (SL) boards play a key role in the new Level-0 muon trigger system. The full system includes 80 SL boards, covering pseudorapidity (eta) range |eta| < 2.4. They receive the hit data of RPCs (barrel, |eta| < 1.05) and TGCs (endcap, 1.05 < |eta| < 2.4) from the on-detector electronics and reconstruct muon candidates. In order to suppress the fake trigger arising from the particles not from interaction point and to improve the momentum determination, the data are combined with the information from NSW and TileCal and the muon candidates are selected. The selected muon candidates are transferred to the boards dedicated for the processing of the MDT hits, where further selection is applied with improved momentum resolution. The SL boards also serve as the readout boards of the RPC and TGC hit data.

Each SL board is designed as an ATCA blade, integrated with Virtex UltraScale+ XCVU13P FPGA, Mercury XU5 MPSoC mezzanine card, and CERN-developed IPMC. FireFly modules provide 120 pairs of transmitters and receivers. Clock is managed with Si5345 chips and fixed latency scheme is employed. Power is supported up to 350 W. The first prototype (attachment 1) of the SL board was produced in Oct. 2021. All the functions of the hardware were demonstrated and confirmed after minor modifications on the produced board.

The trigger firmware will be implemented in XCVU13P FPGA. The track segment reconstruction using TGC hits is a core part of the Level-0 muon trigger for the endcap region, since the track segments constitute the primitive muon candidates and later stages of the Level-0 muon trigger only apply selections. The track segment reconstruction is performed with a pattern matching algorithm, where the TGC hits are compared with predefined hit patterns stored in UltraRAM. Each predefined hit pattern has associated position and angle data of the track segment. The firmware has been developed (attachment 2) for full coverage of the endcap and the performance was evaluated with the post-synthesis simulation. We achieved 1 cm position and 4 mrad angular resolutions with less than 40% of the UltraRAM resources. The latency is within ˜100 ns and the throughput rate is 40 MHz. The efficiency is greater than 95%. The study demonstrates the feasibility of processing the TGC hits from ˜7000 channels within ˜100 ns using single XCVU13P FPGA for muon tracking.

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