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Hardware Design and Testing of the Generic Rear Transition Module for the Global Trigger Subsystem of ATLAS Phase-II Upgrade

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The Global Trigger will bring even-filter-like capability to the High-Luminosity trigger system of the ATLAS experiment. Its several firmware-based nodes will run on identical hardware, the Global Common Module, an Advanced Telecommunications Computing Architecture front board. A matching rear-transition module (RTM), called Generic RTM (GRM) was developed to mitigate risks of complex design and power management. GRM features a Xilinx Versal Prime system-on-chip to communicate
with the FELIX subsystem and trigger processors for readout and system control; a lpGBT chip enables emulation of the detector front-ends. This summary presents the ongoing testing of key functionalities of GRM.

Summary (500 words)

The Global Trigger subsystem will be introduced in the ATLAS experiment's High-Luminosity Large Hadron Collider trigger system, to enable event-filter-like capabilities. Its firmware-based processing nodes will be hosted on common hardware, called Global Common Module (GCM). GCM is an ATCA front board whose complex design, presented at this conference last year, needs to meet the requirements of every node and is close to the maximum power budget. To mitigate the design risks, a matching rear-transition module (RTM), called Generic RTM (GRM) and showed in the figure, was developed as a versatile board which can consume additional 50W and can handle system-control and communication with the Front-End Link eXchange (FELIX) subsystem, and can also emulate detector front-ends for integration tests.

As the block diagram shows, GRM features a Xilinx Versal Prime VM1802 system-on-chip with many dedicated interfaces, DDR4 RAM and 42 25.8 Gb/s multi-gigabit transceivers (MGT): 24 MGTs accessing 2 Tx-Rx pairs of 12-channel FireFly optical modules (for communication with FELIX and other applications) and 18 MGTs connected to the 2 processing FPGAs of the GCM front board (for monitoring, control, and data transmission). A Low-Power GigaBit Transceiver (lpGBT), a radiationhard application-specific integrated circuit, is connected to the VM1802 FPGA via its electrical links (eLinks), while its high-speed links (10.24 Gb/s Tx and 2.56 Gb/s Rx) are handled by a Versatile Link PLUS (VTRx+) radiation-hard optical transceiver.

The major functionalities of the GRM prototype have been being verified since November, so far successfully despite challenges due to new design flows of the Versal chip and its interfacing to the lpGBT. As both devices will play crucial roles in detector readout for long time, this experience will be also valuable to other designs (eg. the next versions of GCM and FELIX hardware). The VM1802's operating system was cross-compiled with PetaLinux, boots via SD, and is accessible through the UART and GbE interfaces. Python scripts perform power-on I2C configuration of clock chips, lpGBT and FireFly modules, as well as monitoring of power consumption and thermal performances. The signal integrity of the transceivers was evaluated with integrated bit-error-ratio tests: firstly, in internal physical-medium-attachment loopback tests on all the 44 MGTs, at both 12.8 and 25.8 Gb/s line-rates; secondly, in external loopback through the 2 Tx-Rx pairs of 14-Gb/s and 25-Gb/s FireFly

optical modules, at 12.8 Gb/s (avg. open area = 7900) and 25.8 Gb/s (avg. open area = 5380) respectively. Tests of lpGBT are ongoing and involve the validation of: configuration of the lpGBT, in transceiver and simplex-Tx modes, via I2C and optical interfaces; eLinks between “Low-Voltage Differential Signaling”pins of the VM1802 and “CERN Low Power Signalling”pins of the lpGBT; high-speed optical links of the lpGBT, between VTRx+ and FireFly modules, ensuring up-link and down-link alignment; complete up-link and down-link loopbacks, with data generation and checking at VM1802 FPGA through eLinks and VTRx+, as shown in the second block diagram (blue being up-link, red down-link). Further progress will be reported at the conference.

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