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An ATCA Processor for Level-1 Trigger Primitive Generation and Readout of the CMS Barrel Muon Detectors

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An ATCA processor was designed to instrument the first layer of the CMS Barrel Muon Trigger. The processor receives and processes DT and RPC data and produces muon track segments. Furthermore, it provides readout for the DT detector. The ATCA processor is based on a Xilinx XCVU13P FPGA, it receives data via 10 Gbps optical links and transmits track segments via 25 Gbps optical links. The processor is instrumented with a Zynq Ultrascle+ SoM connected with an SSD which provides for enhanced monitoring and control information. The design of the board as well as results on its performance are presented.

Summary (500 words)

The first layer of the CMS Barrel Muon Trigger Level-1 consists of 60 ATCA boards which receive data from the Drift Tube (DT) and Resistive Plate Chamber (RPC) detectors in the CMS barrel region via optical links running at 10 Gbps using the LpGPBT protocol. The CMS Barrel Muon DT detector is segmented in 60 sectors (12 wedges in the φ direction × 5 sections in the theta direction). A sector is instrumented with 4 planes of DT chambers and the corresponding RPC layers. The data arrives in the form of muon hits and the ATCA boards processes them to produce track segments/stubs. Each station can produce up to 4 stubs. The stubs are transmitted via 25 Gbps links to the CMS GMT. Additional information regarding the quality of each stub along with information about the data used to produce it are also produced and are transmitted to GMT. GMT processes the stubs using a KALMAN algorithm to search for muon candidates in the barrel region and reconstructs for each candidate the transverse momentum, the pseudorapidity, the azimuthal φ angle, the charge, along with information regarding the origin of the muon (primary or a secondary vertex) as well as other quantities for each muon candidate.

The ATCA processor is instrumented with a Xilinx XCVU13P-FLGA2577E FPGA (interchangeable with XCVU11P and XCVU9P) which was chosen based on the current size of the algorithm firmware which reconstructs the stubs as well as the number of DT and RPC links. The technical characteristics of the FPGA are 1728000 LUTs, 3456000 FF, 12228 DSPs, 128 GTY Transceivers, 94.5 MB Block RAM and 360 MB UltraRAM. The ATCA Processor is instrumented with 20 Samtec Firefly optical modules which are configured as follows: 40 × Rx links at 25 Gbps, 40 × Tx links at 25 Gbps, 80 × Rx links at 16 Gbps, 36 × Tx links at 16 Gbps. The total input and output data rates are 2.28 Tbps and 1.58 Tbps respectively. The onboard clocking network supports both synchronous and asynchronous operation for each transceiver quad independently and arbitrary frequency synthesizing. A ZYNQ Ultrascale+ System on Module (Enclustra Mercury XU-5) connected to an SSD provides for control and enhanced monitoring capabilities. An SD card is also connected to the ZYNQ. The ZYNQ communicates with the FPGA via four GTH transceivers and is accessible vie USB 3.0, DisplayPort, UART and Gbit Ethernet facilitated by an onboard Gbit Ethernet switch.

Each of the ATCA processors can serve one or two sectors depending on the algorithm firmware size. An algorithm model in VHDL has been developed and according to this the algorithms from two sectors could comfortably fit in one ATCA board. However, for firmware contingency reasons, we currently plan that each ATCA processor processes the data from only one sector.

Results on the processor performance along with measurements which characterize the board optical communications, its power system and power dissipation are presented.

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