Contribution ID: **13** Type: **Oral**

New developments in the MDT Trigger Processor for the ATLAS Level-0 Muon Trigger at the HL-LHC

Tuesday, 20 September 2022 14:40 (20 minutes)

The MDT Trigger Processor (MDTTP) processes muon trigger candidates along with Monitored Drift Tubes (MDT) hits to improve the accuracy of the transverse momentum calculation at the first-level (level-0) of the muon trigger. The challenge would be processing all candidates in a bunch crossing to meet latency requirements of High-Luminosity LHC. The MDTTP hardware is based on the Apollo ATCA platform. A complete hardware demonstrator is available and an updated prototype has been recently developed. We present here the progress on hardware and firmware development along with recent performance studies from simulations.

Summary (500 words)

The Level-0 Muon Trigger System improves the muon trigger selectivity (efficiency turn-on) and allows to keep the single muon trigger rate under control by suppressing the fake muon triggers in the high luminosity era. The MDTTP defines region of interest (RoI) using limited resolution track coordinates from the existing Sector Logic (SL) processors. Track segments are formed using MDT hits within the RoIs in the different MDT stations and are then combined to provide a transverse momentum measurement with a resolution close to the one achieved in the ATLAS offline muon reconstruction.

The MDTTP hardware is based on the open source Apollo ATCA platform, which comprises a common Service Module (SM), an application-specific Command Module (CM), in addition to a firmware and software toolkit. The SM provides power conditioning, clock and communication infrastructure, support for a CERN-compatible IPMC, and a System on Module. The MDTTP CM implements the muon trigger candidate reconstruction with all the optical interfaces, local clocking and slow monitoring infrastructure. The demonstrator, first version of the MDTTP CM, was manufactured with two programmable logic devices and optical interfaces up to 25 Gbps. The prototype version uses a single FPGA and simplifies firmware and board design.

The CM MDTTP firmware is designed to have a fixed latency of approximately 1.7µs and is divided into Hardware Abstraction Layer (HAL) and User Logic (UL). The HAL firmware implements the low level interface to SL, Chamber Service Module (CSM) of the MDT front-end electronics, SM and FELIX, providing control and data to UL at 320MHz clock frequency. The UL firmware implements the trigger, data acquisition, control and monitoring logic. The trigger path logic, receives the muon trigger candidate from the SL, implements a refined measurement of its properties based on MDT hits and sends it back to SL subsystem for the final muon trigger decision. The data acquisition logic responds to L0 accept signals at 1MHz rate and sends the MDT hit information to ATLAS DAQ for storage. The control logic helps with firmware configuration during reset and run time while the fast monitoring logic provides real- time information about the data quality and trigger algorithm.

The UL firmware block integration and functional validation require test vectors from offline simulation and test infrastructure to simulate the firmware. To enable the parallel firmware design and test infrastructure development, centralized data formats have been defined for all CM firmware block interfaces. The test framework developed includes generation of test vectors from offline simulation, for a given bunch crossing test vectors are generated for all the firmware block interfaces This allows for testing a single firmware block, chain of blocks or the entire trigger path. This helps with comparing firmware performance plots against offline simulation and provides infrastructure to break down and debug logic data paths.

In this paper we present the status of the CM hardware, firmware , testing and validation status. Muon trigger performance studies using the simulated MDTTP algorithms will also be included.

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Session Classification: Trigger

Track Classification: Trigger