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DESIGN AND CHARACTERIZATION OF A CASCODE SWITCHING STAGE FOR HIGH FREQUENCY RADIATION HARDENED DC/DC CONVERTERS FOR THE SUPPLY OF FUTURE PIXEL DETECTORS

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Introduction: Serial Powering features the upcoming phase II HL-LHC upgrade in the ATLAS and CMS experiment. The conventional voltage based powering approach with parallel placed modules results in low powering efficiency. In addition restricted space requirements, radiation tolerance and high magnetic fields makes the design of a suitable DC/DC-converter challenging. To ensure that future DC/DC converters can tolerate high radiation doses at reduced space requirements, a high-frequency switching stage with up to 4 stacked core devices with a related biasing circuit for the implementation in DC/DC-converters was considered and successfully verified in a first prototype.

Parallel powering

The increased number of pixels in the upcoming phase II upgrade of the ATLAS and CMS pixel detectors leads to a higher power consumption of the overall detector. At constant module voltage, the supply current across the long cables increases and leads to higher I^2R losses. To avoid a degradation of the overall system efficiency new powering concepts were established.

Serial Powering:
- The serial powering concept was chosen as the baseline option for the upcoming upgrade
- Several modules were connected in a serial chain and supplied with a constant current
- A ShuntLDO regulators is used to converter the supply current in a constant voltage
- Redundancy is integrated in order to prevent the entire chain from crashing if one regulator fails

Parallel Powering with DC/DC conversion:
- Several modules are connected in parallel, like in figure 1
- Efficiency improvement is achieved by distributing power and increasing supply voltage and thus lower supply current. A DC/DC converter reduces the voltage to the desired level close to the module
- A module failure does not affect the entire module group
- **A short chain serial powering will be used for 3D sensor modules in the innermost layer [4]**
  → **Less effort and higher robustness using a parallel concept for 3D sensor modules**

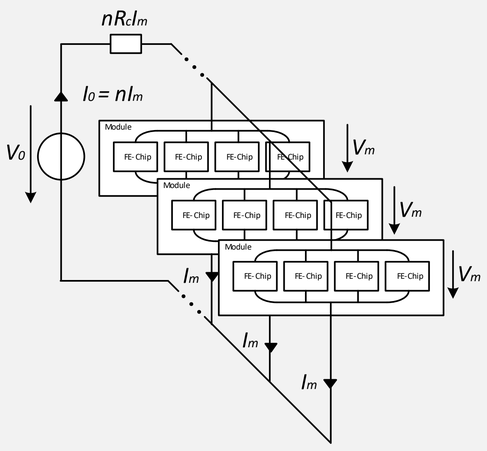

Figure 1: Pixel modules connected in parallel

DC/DC- converter requirements

The following requirements are specified for the implementation of a practical DC/DC converter in the harsh environment of the detector:

- A **total ionizing dose of up to 1 Grad** should be tolerated
  → To achieve the requirements of radiation hardness, the whole converter should be designed with low voltage core transistors of a 65nm TSMC CMOS technology
- For the realisation of short module chains, a **voltage conversion factor of 4** is targeted (the input voltage is 4 times higher than the module voltage)
  → In order to comply the voltage limits of the core devices, it is necessary to stack the switching stage with a minimum of 4 transistors
- **Space requirements**: Because of the high magnetic field inside the detector the inductor cannot be designed with a ferromagnetic core. **Only bulky air coils** can be used.
  → To meet the space requirements, the inductance has to be reduced to decrease the volume of the inductor. This is achieved by operating the DC/DC-converter at **high switching frequencies (Multi MHz)**

Device stacking

Figure 2 shows a cascode switching stage with 4 NMOS and PMOS devices each. The circuit is able to sustain four times the nominal supply voltage. The switching state of the cascode stage is controlled via a signal of a feedback system and the PMOS and NMOS stage is conducting alternately.

- VDD = Nominal voltage of core devices
- Max. Voltage of core devices: 1.1X(nominal voltage)
- **To guarantee a long life time the voltage limits should not be exceeded**

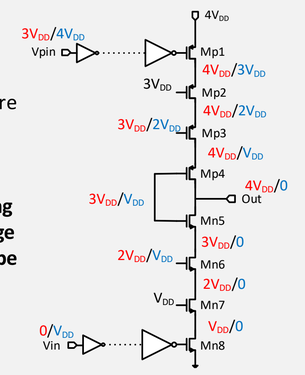

Figure 2: Cascode switching stage

Cascode switching stage (submitted testchip)

A cascode switching stage built with up to 4 stacked transistors was tested in a first prototype and characterized for application in a high frequency DC/DC converter. The circuitry, shown in figure 3, was originally used in [1] for the implementation of an xDSL driver.

- The circuit alternates between two switching states:
  → **HIGH State** (V_x is charged to 4VDD)
  → **LOW State** (V_x is discharged to ground)
- **Only two control signals** are necessary (Vin & Vpin)
- Biasing devices Mbn1 – Mbn3 and Mbp1 – Mbp3 provides the required voltages at the gates of the remaining cascode devices depending on the switching state
- The **functionality was tested** and **verified** in a first prototype (65nm TSMC)
- The switching stage was tested with different frequencies in the Multi MHz range, see figure 4 and 5
  → Ringing occurs due to parasitic effects of the cables and the PCB
- **Simulation results show large voltage peaks during switching moment** (fig. 6 and 7)
  → Will lead to **hot carrier effects** and which will reduce device life time

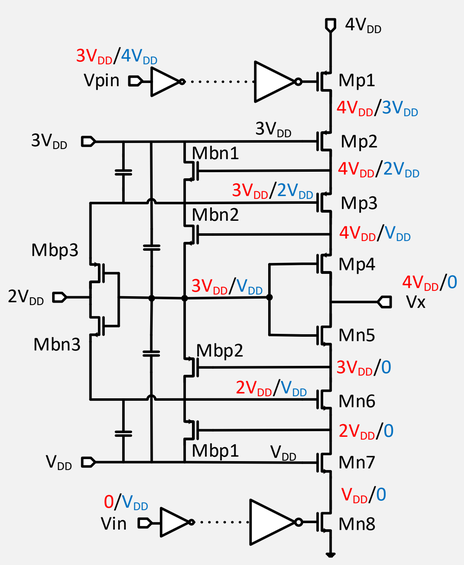

Figure 3: Cascode switching stage with biasing devices [1]

Figure 4: Measurement result (20 MHz)

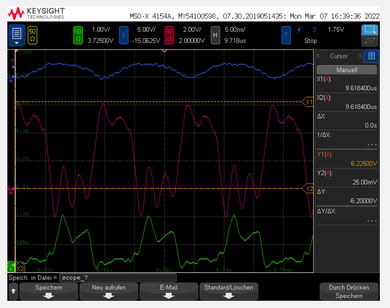

Figure 5: Measurement result (80 MHz)

Voltage peaks during switchinig action

Figure 6 shows transient simulation results of the drain source and gate source voltages of devices Mp1 – Mp4 and Mn5 – Mn8.
→ During the switching moment high voltage peaks occur (red dotted line indicates the boundary limit)

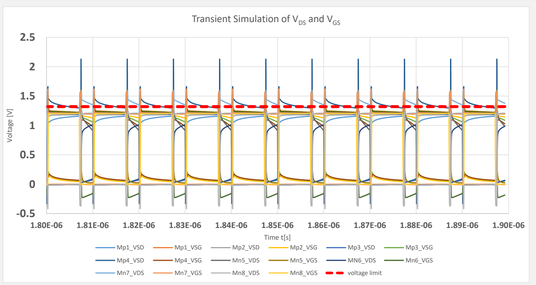

Figure 6: Transient simulations of VDS and VGS voltages

Figure 7 shows a vgs vs vds plot for both stages where dotted red line presents the save area → Siginificant limit exceedances can be seen which will lead to hot carrier effects

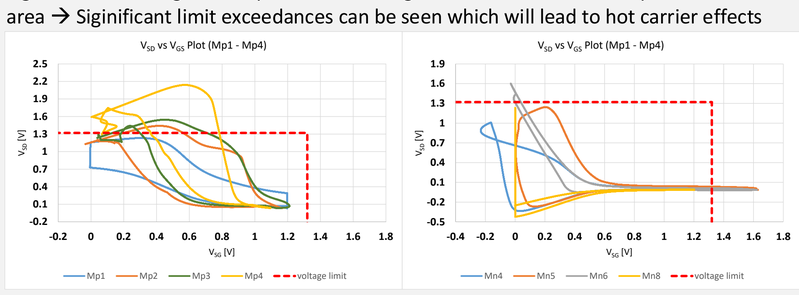

Figure 7: VDS vs. VGS plot. Left: PMOS stage. Right: NMOS stage

Improved cascode stage

Many proposed cascode switching stages from literature suffer from voltage peaks during switching moment. Since the cascode stage behaves different with an inductive load, not every concept from the literature is appropriate for the application in a DC/DC converter. A new concept is introduced where the influence of the inductor as load is also taken into account. Improvements have been made so that no voltage limit violations longer occur. This eliminates the hot carrier effects and extends the life time of the devices.
The new concept is shown in figure 8. Five control signals are required to control the circuitry. Therefore, a non overlapping clock generator was integrated [3], see figure 11. Since a voltage swing of 2VDD is required to drive the transistor gates Mp4 and Mn5, a two stage buffer concept was implemented [2]. In order to raise up the control signals, capacitive floating level shifters are used. The gates of the stacked transistors are driven via tapered buffers. Figure 9 shows simulation results and proves that all transistors keep their limits with the new concept. The critical situations where voltage overshoots can occur and the proposed solutions with the new concepts are presented:

1) NMOS Stage – Transition from LOW to HIGH: If Mn8 switches into the cut off region its drain potential rises to VDD – VTH until Mn7 switches off. Because of the subthreshold effect the drain potential of Mn8 is slowly charged to VDD. This effect also occurs for the drain of devices Mn7 and Mn6. The drain of Mn5 is charged to 4VDD via the PMOS stage. The slow charging to the final voltage level leads to voltage peaks of VDS and VGS.
→ **Solution:** The additional devices Mdp1 – Mdp3 are added to charge the drain nodes of the cascode stage quickly to the finale value and eliminates the voltage peaks.

2) PMOS Stage – Transition from HIGH to LOW: The same procedure as described in section 1) for the PMOS stage.
→ **Solution:** Mbn1 – Mbn3 were added to charge the drains quickly to their final value

3) NMOS Stage – Transition from HIGH to LOW: As soon as the NMOS stage gets activated all drain potentials of Mn5 – Mn8 are discharged to ground. If the drain of Mn7 is still at 2VDD and Mn8 switches on, its drain is discharged to ground. Mn7 gets active if the drain of Mn8 is at VDD – VTH. This will lead to an voltage overshoot of one threshold voltage. This effect also occurs for the other devices.
→ **Solution:** Before the NMOS stage gets active a pre-discharge of the drain nodes are necessary: This is achieved in a natural way with the help of the inductor and a small dead time between the control signals. Since the inductor has stored energy for each load cases during this transition, the inductor forces the current flow by discharging the drain nodes of the NMOS stage, so that Mdp1 – Mdp3 becomes conductive sequentially and supply the inductor → Pre-discharge avoid voltage peaks.

4) PMOS Stage – Transition from LOW to HIGH: To prevent the circuit from over voltage scenarios that could occur when the PMOS stage gets on, it is necessary to pre-charge the drain nodes of this stage before Mp1 becomes conductive.
→ **Solution:** During the dead time a pre-charging process occurs because of the stored energy of the inductor together with the additional devices.

5) NMOS Stage – Dead Time: During the transition from HIGH to LOW there is typically a small dead time before Mn8 switches on. If the dead time is chosen too large the body diode of Mn8 gets conductive and all drain nodes are negatively discharged to form a conductive path from the NMOS stage to the inductor even if the control signal is off. This leads to significant exceedances of the voltage limits.
→ **Solution:** The additional devices (Mdp1 – Mdp3) of the NMOS stage getting active during the dead time and provide a current path for the inductor. This avoids a negative discharge of the drain nodes.

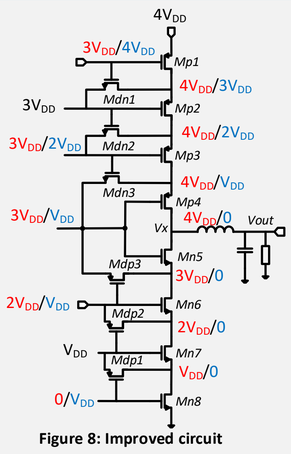

Figure 8: Improved circuit

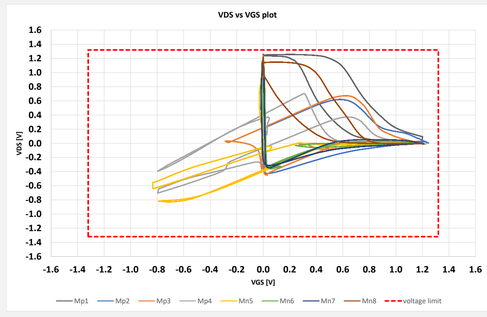

Figure 9: VDS vs VGS plot of Mp1 – Mp4 & Mn5 – Mn8 for improved circuit

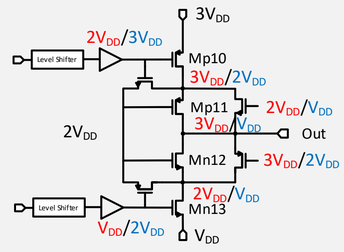

Figure 10: Circuit to generate a control signal with a voltage swing of 2VDD [2]

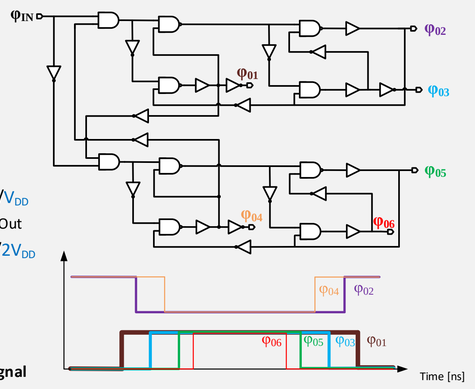

Figure 11: Six phase non overlapping clock generator [3]

Improved switching transition from HIGH to LOW

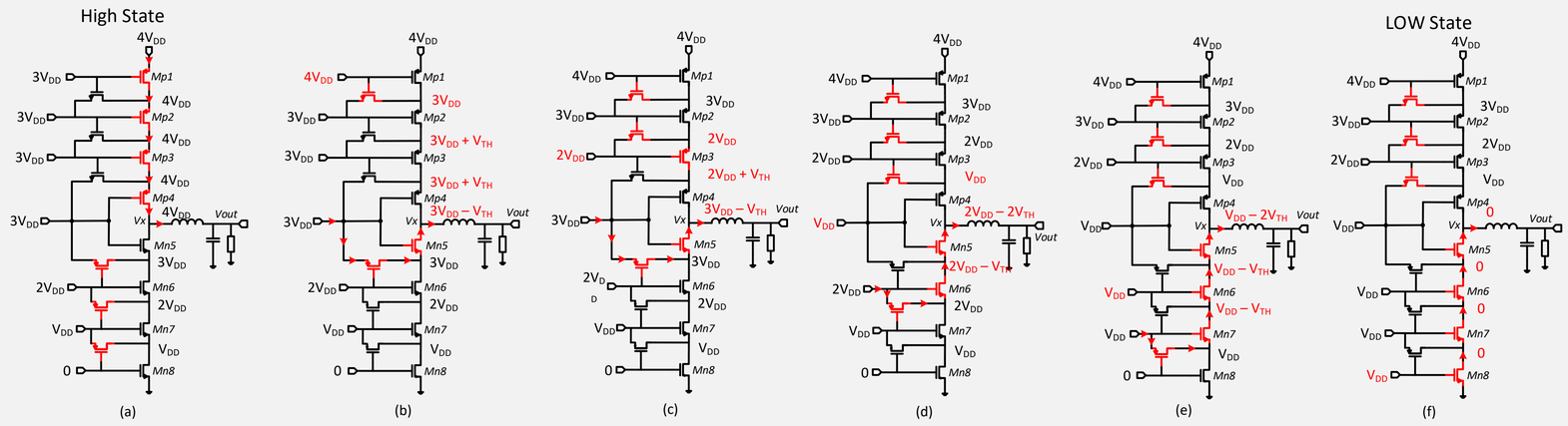

Figure 12: The circuit switches from the HIGH state to the LOW state. The direction of the current flow is shown with red arrows. Conducting devices are highlighted in red

Improved switching transition from LOW to HIGH

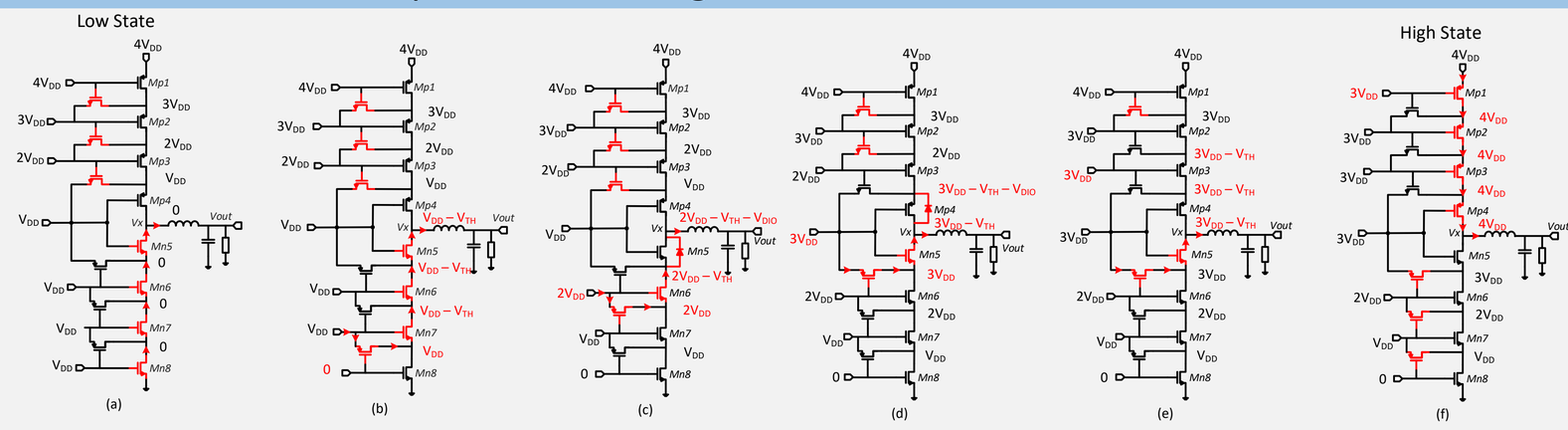

Figure 13: The circuit switches from the LOW state to the HIGH state. The direction of the current flow is shown with red arrows. Conducting devices are highlighted in red

References

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