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Design and characterization of a cascode switching stage for high frequency radiation hardened DC/DC converters for the supply of future pixel detectors

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Serial Powering features the upcoming phase II HL-LHC upgrade in the ATLAS and CMS experiment. The conventional approach of placing the pixel modules in a parallel arrangement could not be established due to different limitations like restricted space requirements or radiation tolerance, which makes the design of a suitable DC/DC-converter challenging. To ensure that future DC/DC converters can tolerate high radiation doses at reduced space requirements, a high-frequency switching stage with up to 4 stacked core devices with a related biasing circuit for the implementation in DC/DC-converters was considered and successfully verified in a first prototype.

Summary (500 words)

An efficiency improvement for the parallel arrangement of the pixel modules can be achieved by increasing the supply voltage across the long cables and decreasing the voltage to the desired module level by a DC/DC conversion. This will decrease the supply current and therefore the Iˆ2R losses and will lead to an efficiency improvement of the detector system. For the serial arrangement of the pixel modules, there is a risk that the failure of one module will affect the entire chain. To avoid this, additional measures have to be performed to ensure a safe operation. This problem does not occur for a parallel connection, since the modules are independent of each other. The DC/DC converters that enable the parallel concept have to withstand a high radiation dose. Therefore, low voltage core devices are favoured due to their strong radiation resistance. Since the nominal voltage of these devices is low the transistors have to be stacked in order to tolerate high supply voltages at the input. A cascode switching stage built with up to 4 high side and 4 low side devices was analysed and tested. With an arrangement of 4 the switching stage could lead voltages that are 4 times higher than the nominal voltage of the transistors. A biasing circuit was examined which is necessary to operate the stacked transistors within their voltage limits and provides the required voltages to the stacked transistors depending on the switching state. The design procedure and the methods for the usage of the stacked stage in a DC/DC converter are presented.

A first prototype produced in a 65nm technology was characterized and investigated. The functionality of the prototype was proven and is ready to be tested during irradiation. The implementation of low voltage core transistors does not only result in a high radiation tolerance, the losses can also be kept smaller compared to using HV devices. Due to the high magnetic field inside the experiments, the magnetic components of the DC/DC converters can only be implemented with air coils. Since the air core inductors have a larger volume compared to their counterpart built with magnetic cores, a multi-MHz operation is recommended to decrease the needed inductivity. Therefore, the switching stage was also successfully tested for multi-MHz operation. A drawback of the circuit is, that it suffers from hot carrier effects due to transient voltage overshoots during the switching moment. This effect can reduce the lifetime of the devices. To overcome this issue, concepts are presented that show an improved behaviour and will be investigated in future prototypes.

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