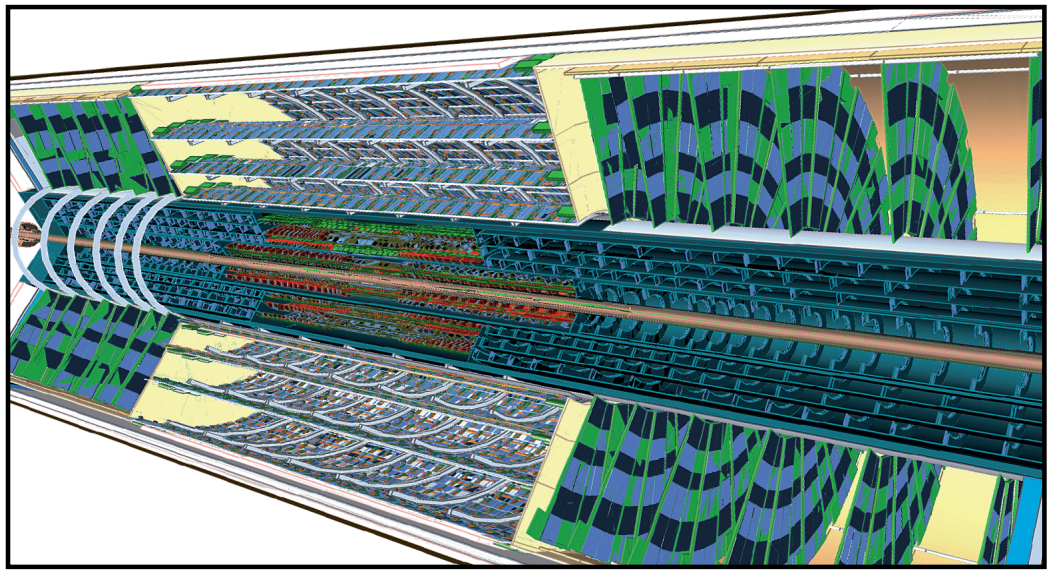
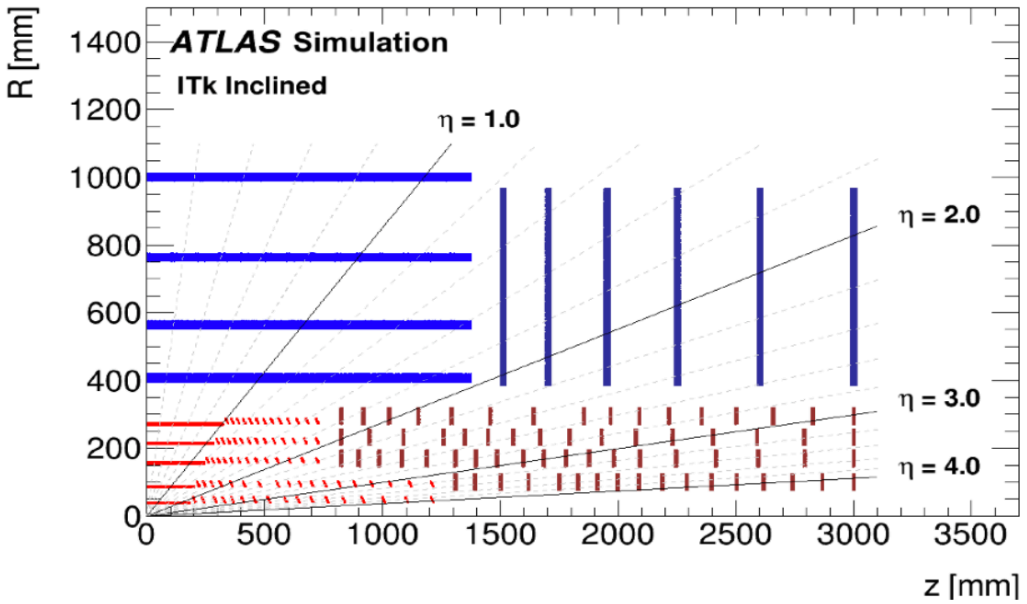
Electrical performances of pre-production staves for the ATLAS ITk Strip Detector Upgrade

Francesca Capocasa for the ATLAS ITk Strip Collaboration

ITk Layout



http://cdsweb.cern.ch/record/2257755/files/ATLAS-TDR-025.pdf



For the HL-LHC, an all-silicon Inner Tracker (ITk) will replace the current ATLAS inner detector

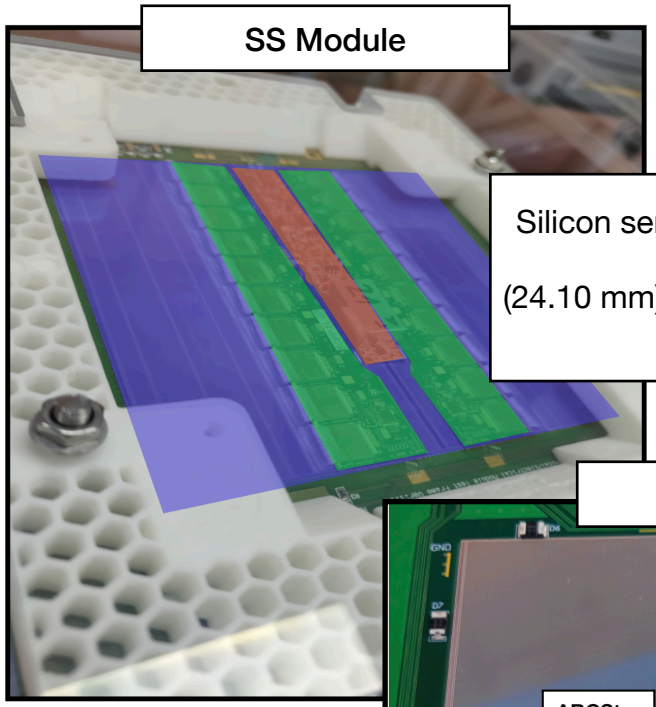
- ITK Pixel Detector
  - 5 barrel layers with inclined sensors in the forward region
  - End-Cap (EC) system containing individually located rings
- ITK Strip Detector
  - 4 barrel layers
  - 6 EC rings on both forward regions

Brookhaven National Laboratory and Rutherford Appleton Laboratory responsible for assembling and testing the ITK's Strip Barrel Detector building blocks, the staves

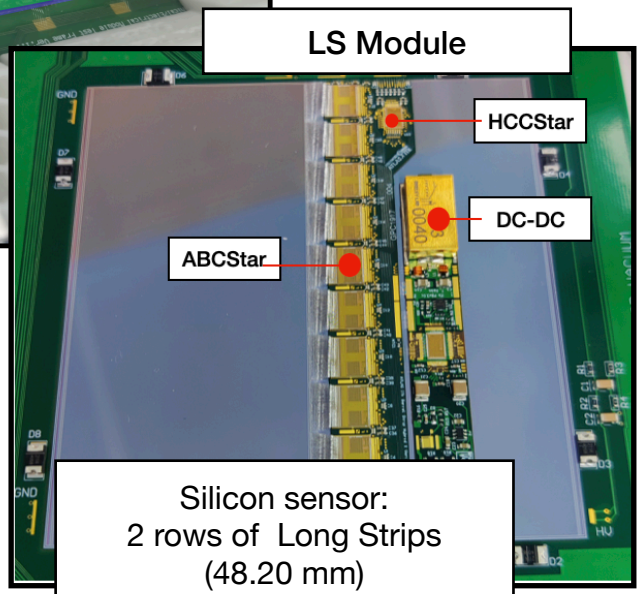
ITk Strip Modules

- The units of the staves are the silicon modules
  - 2 module variant for ITk Barrel Detector having same architecture but different strip length
- Consists of one sensor and one or two low mass PCBs, called hybrids, and one power board

- The hybrid hosts the readout ASICS:
  - 10 front-end ABCStar chips and a control chip HCCStar
  - Each ABCStar has a binary architecture, 256 channels of trimmable preamplifier, discriminator and control logic
  - Each ABCStar has a point-to-point 160 Mbit/s data path to the HCCStar, enabling fast readout



Silicon sensor: 4 rows of Short Strips
(24.10 mm) for higher occupancy regions



Silicon sensor:
2 rows of Long Strips
(48.20 mm)

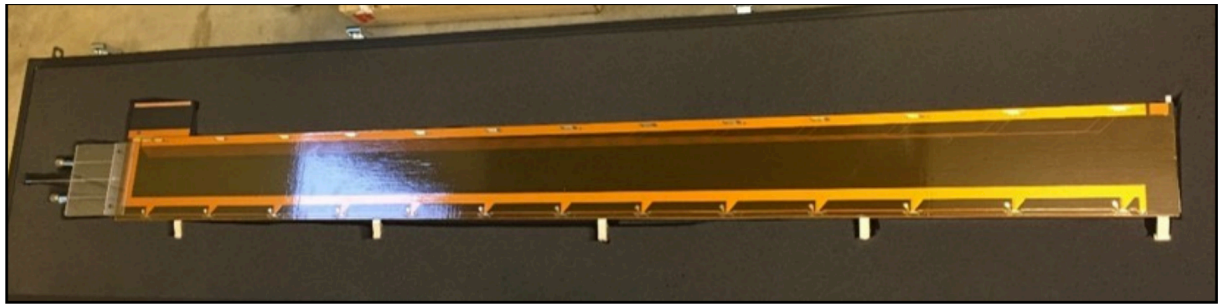
- Power board:
  - Hosts a DC-DC buck converter to step down the LV to 1.5 V used by front-end ASICs
  - Hosts AMAC Chip for Control and Monitor functions:
    - Monitor the sensor HV bias return current
    - Monitor NTC temperatures on hybrids and powerboard

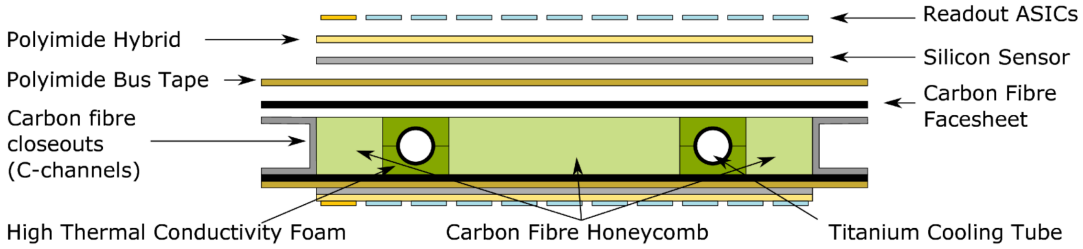
- Radiation tolerance studies of the HV-Mux GaN FETs for the HL-LHC ATLAS ITk Strip Detector - Luis Felipe Gutierrez Zagazeta
- Testing of the HCC and AMAC functionality and radiation tolerance for the HL-LHC ATLAS ITk Strip Detector- Luis Felipe Gutierrez Zagazeta

- Simulated verification of the ASIC functionality and radiation tolerance for the HL-LHC ATLAS ITk Strip Detector - Jeff Dandoy - **link**
- Production and testing of the Powerboards for the ATLAS ITk Strip Barrel Modules - Zhicai Zhang - link

ITk Stave

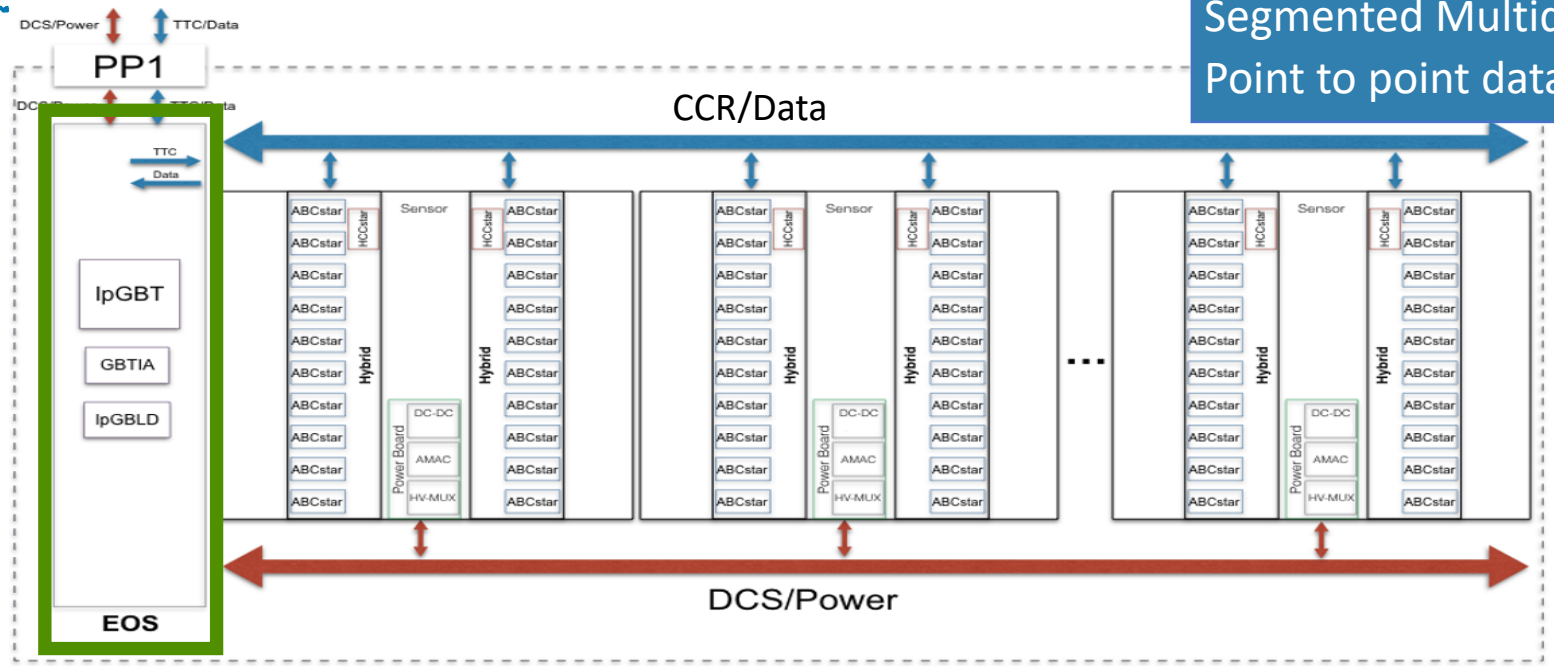
- Staves are the building blocks of the ITk Strip Barrel detector, which provide mechanical support for the modules and host the common electrical, optical and cooling services





- Sandwich geometry:
  - 1.4 m long support structure (stave core)
    - provides **mechanical rigidity and support** by using high stiffness and high thermal conductivity carbon fiber
    - Embedded **cooling** with evaporative CO2
    - Large area copper/kapton co-cured bus tape mounted on both side of the support structure routing electrical services from and to modules
  - 14 silicon modules are directly glued on both sides of the stave support structure with a stereo angle of 26 mrad

Stave Schematics



Segmented Multidrop CCR @ 160 MHz
Point to point data at 640 Mbit/s

LV power bus at 11V
4 HV lines at 500 V
Common LV/HV return
AMAC control and data

Electrical power (LV and HV), CCR (Clock, Control and Reject) data, DCS (Detector Control System) data and measured data transfer services carried out by a copper/kapton bus tape and operated by the EoS (End of Substructure) card

- End of Substructure (EoS) Card
  - Links the off-detector system (electrical, optical) to the stave
  - Contains a radiation-hard optical link (VTRX+) and a data transceiver and serializer (lpGBT)

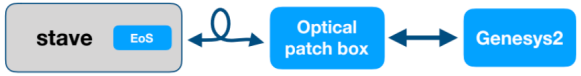
- Bus Tape
  - Responsible of the signal transmission between EoS and HCCStar
  - CCR signals and data
  - Power & AMAC Control and Data

•Current status of the End-of-Substructure (EoS) card project for the ATLAS Strip Tracker Upgrade using final ASICs - Peter Goettlicher

BNL Staves Testing Setup

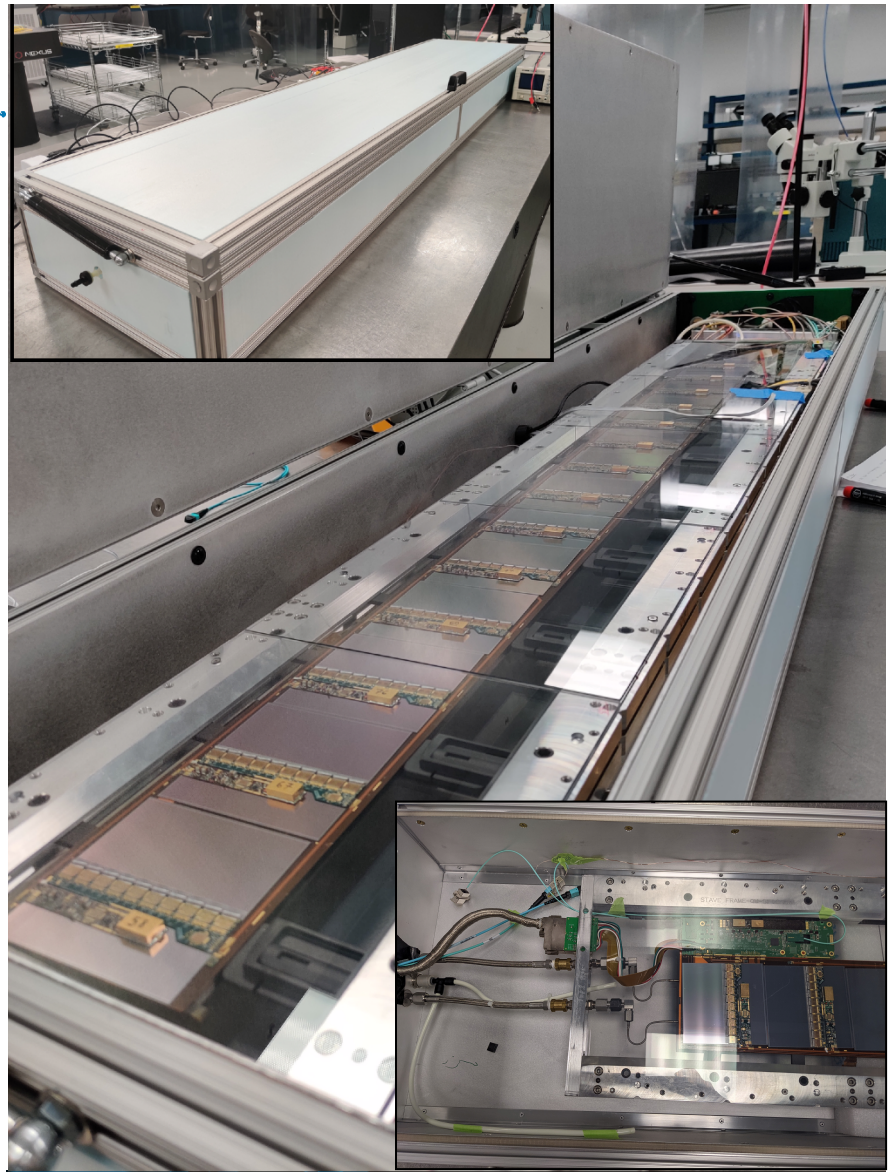
- To facilitate thermal cycling and electrical tests at expected operating temperature, electrical tests are carried out in a cold box
  - Detector will run cold in the experiment to reduce sensor current due to radiation damage
- Slow control implemented: two humidity sensors (SHT85) and two temperature sensors (NTC 10k) readout by a Raspberry pi, monitored with GRAFANA
- Dry air flushing ~ 20 SCFH
- SPS chiller + high pressure booster pump

$T_{chiller}[°C]$	$T_{inlet}[°C]$	$T_{outlet}[°C]$	Pressure[PSI]
35	39.0	40.9	140
30	34.4	36.8	133
20	25.2	28.4	123
10	15.9	20	112
0	7.0	11.0	105
-10	-1.7	4.1	102
-20	-10.5	-4.0	101
-30	-19.4	-12.1	100
-40	-28.5	-20.3	100
-50	-28.7	-20.8	100
-55	-37.7	-28.9	102
-60	-42.4	-33.1	103



- lpGBT programmed via fiber
- Data readout by an FPGA (Genesys 2) , connected to a PC through Ethernet

- For stave QC we are targeting T stave = average (T_{inlet}, T_{outlet}) = -35 C

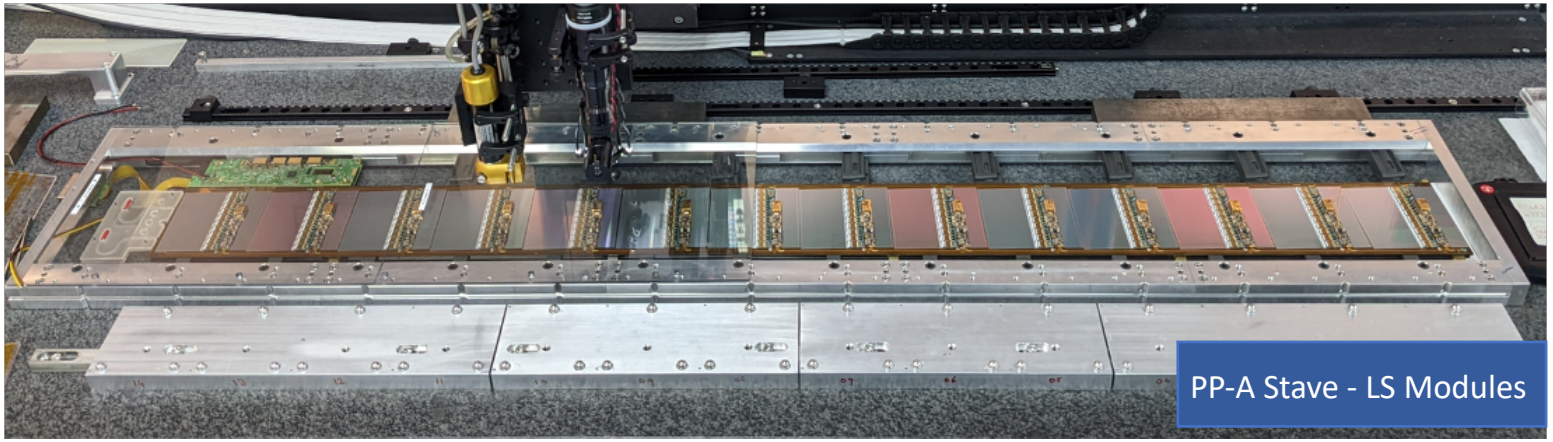


BNL Pre-production staves

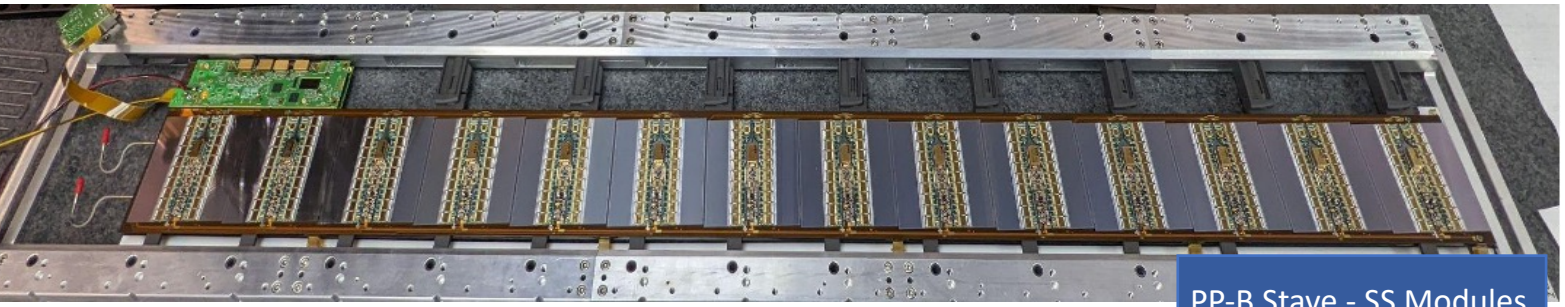
Pre-production(PP) phase consists of two stage process due to part availability:

- PP-A with ~20% of production components,
- PP-B with final components.

Two staves have been assembled at BNL during pre-production phase: 1 PP-A stave and 1 PP-B stave



PP-A Stave - LS Modules



PP-B Stave - SS Modules

What's the difference?

PPA Stave:

- Long Strip Stave
  - Master Side fully populated with 14 LS modules
  - Slave side populated with 4 modules (3 LS and 1 SS)
- Final version of front-end ASICs ABCStar v.1 ✓
- Not final version of HCCStar (HCCStar v0) ✗
- Not final version of AMAC (AMACv2a) ✗

PPB Stave:

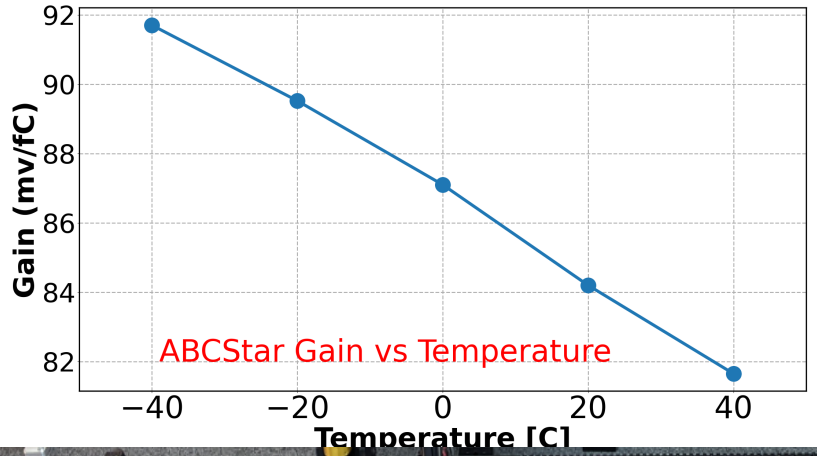
- Short Strip Stave
  - Master Side fully populated with 14 modules
- Final version of front-end ASICs ABCStar v.1 ✓
- Final version of HCCStar (HCCStar v.1) ✓
- Final version of AMAC (AMACStar) ✓

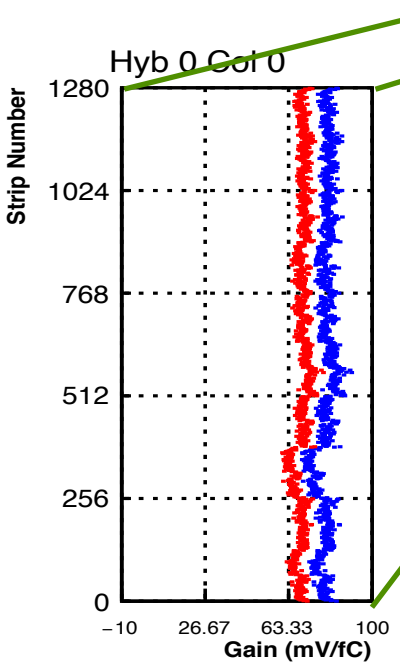
Results Pre-production A stave

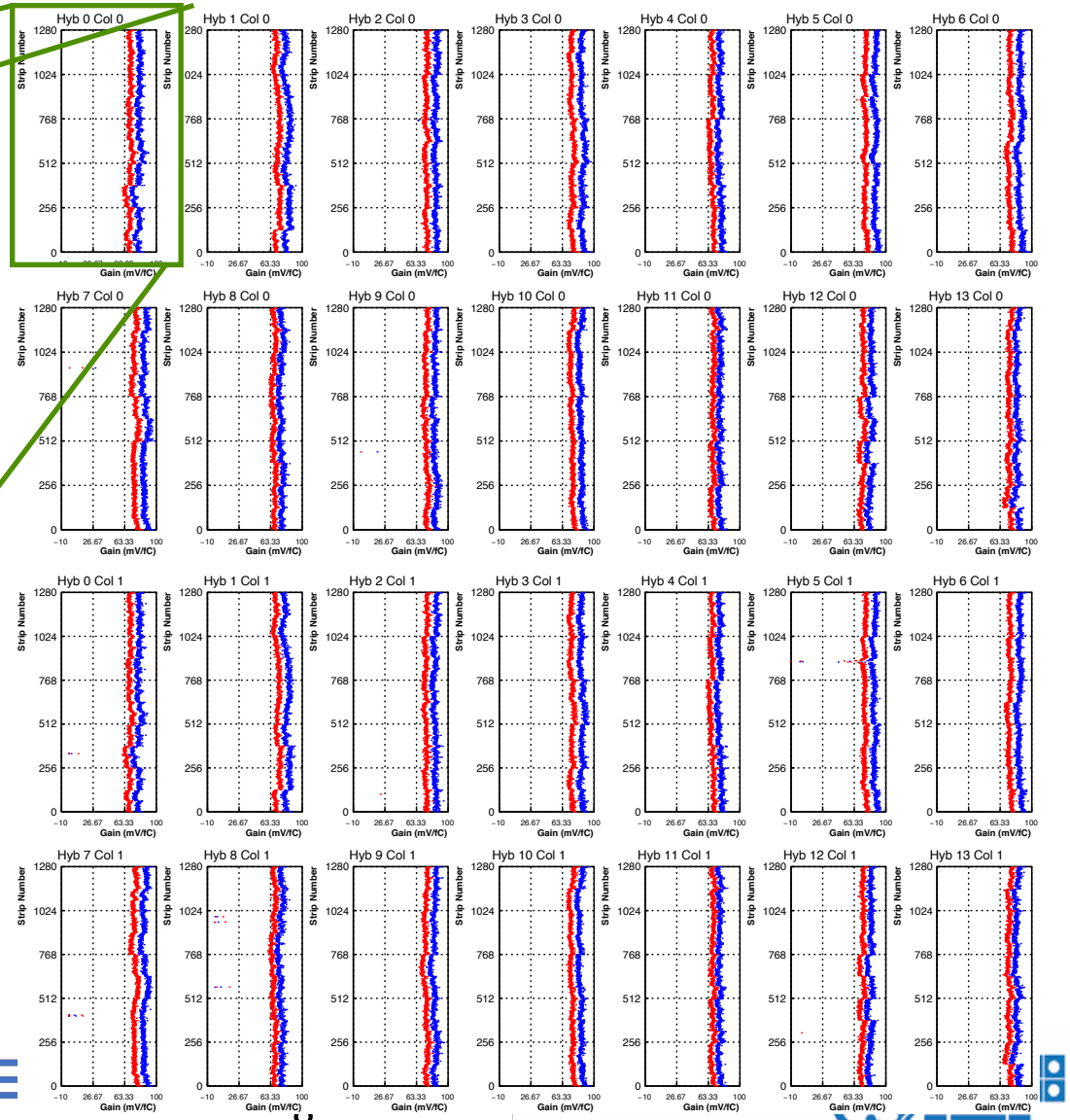
T_{inlet} = 22.3 C, -36.2 C

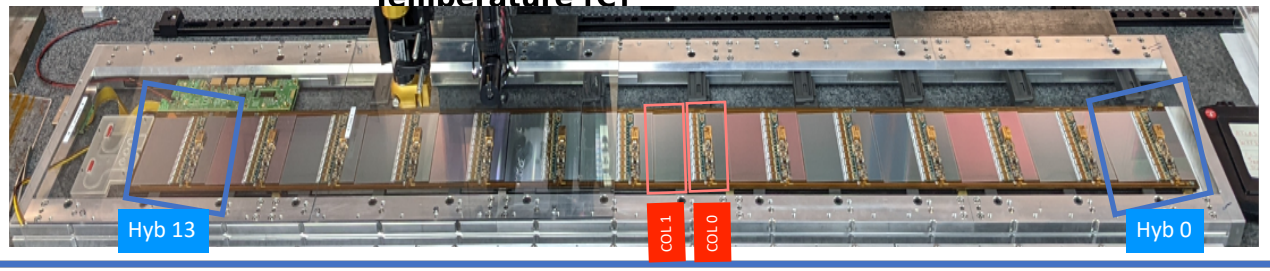
V_{bias} = - 400 V

- Gain response for the 14 LS modules on the one side of the stave
- Gain analyzed independently for the 2 rows of strips of LS modules
- Confirmed ABCStars gain dependencies upon temperature









Results Pre-production A stave

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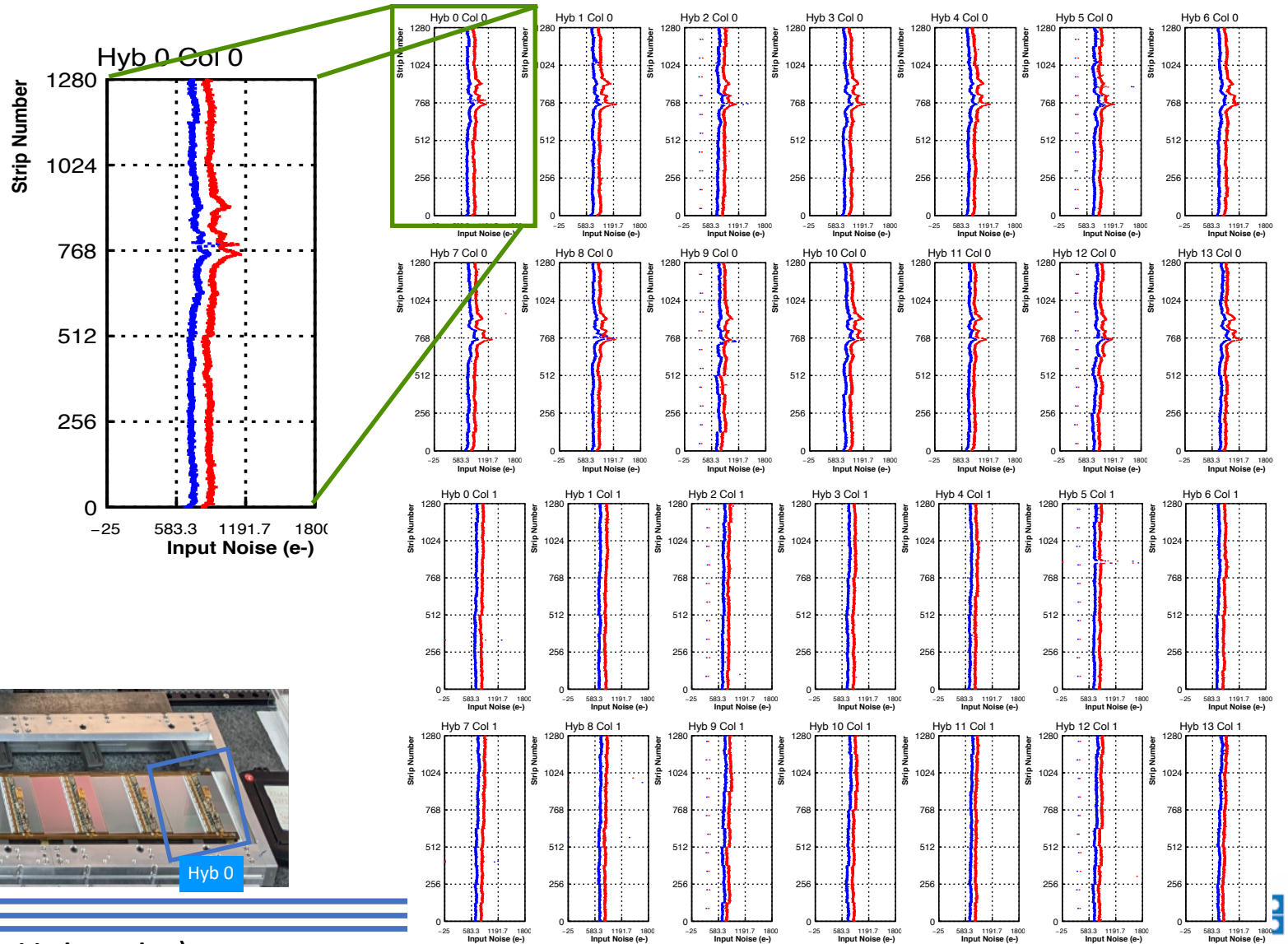
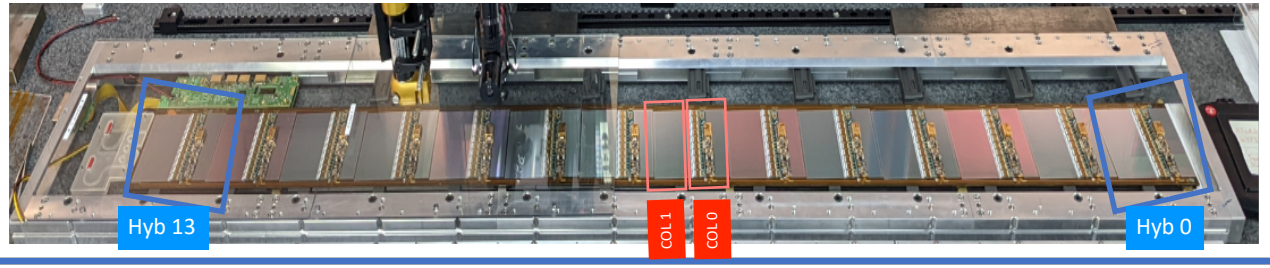
- Input Noise response for the 14 modules on one side of the stave
- Input Noise analyzed independently for the 2 rows of strips of LS modules

- Left 1 unbounded channel for ABCStar on BNL modules as investigative tool
- Good noise performance !

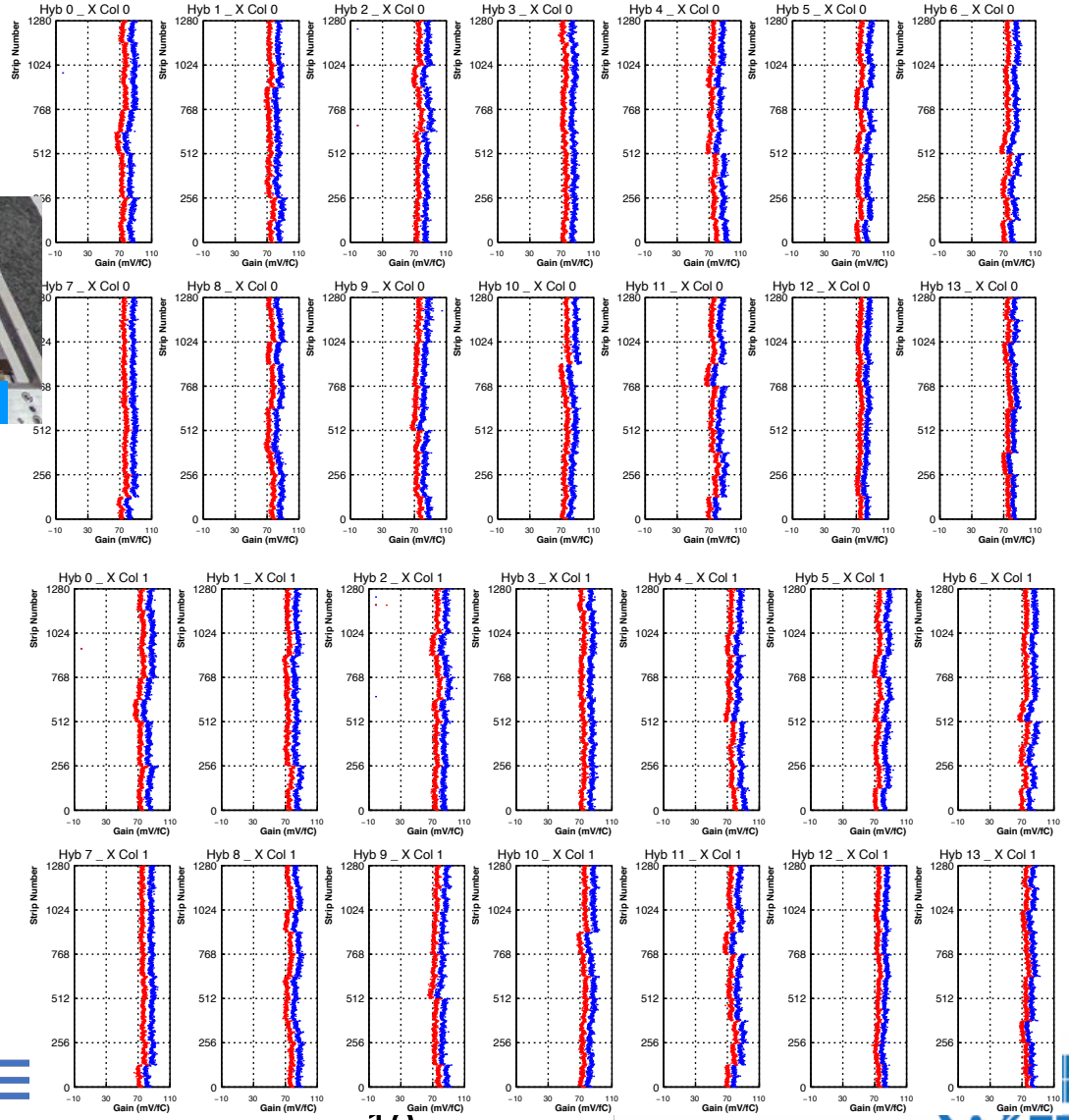




Results Pre-production B stave

T_{inlet} = 24.9 C, -40.5 C

V_{bias} = - 400 V



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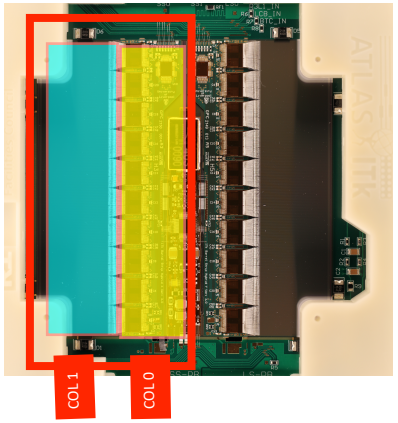

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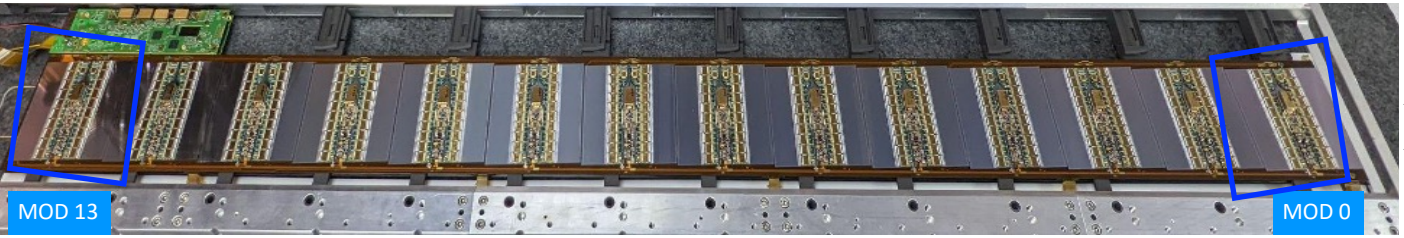

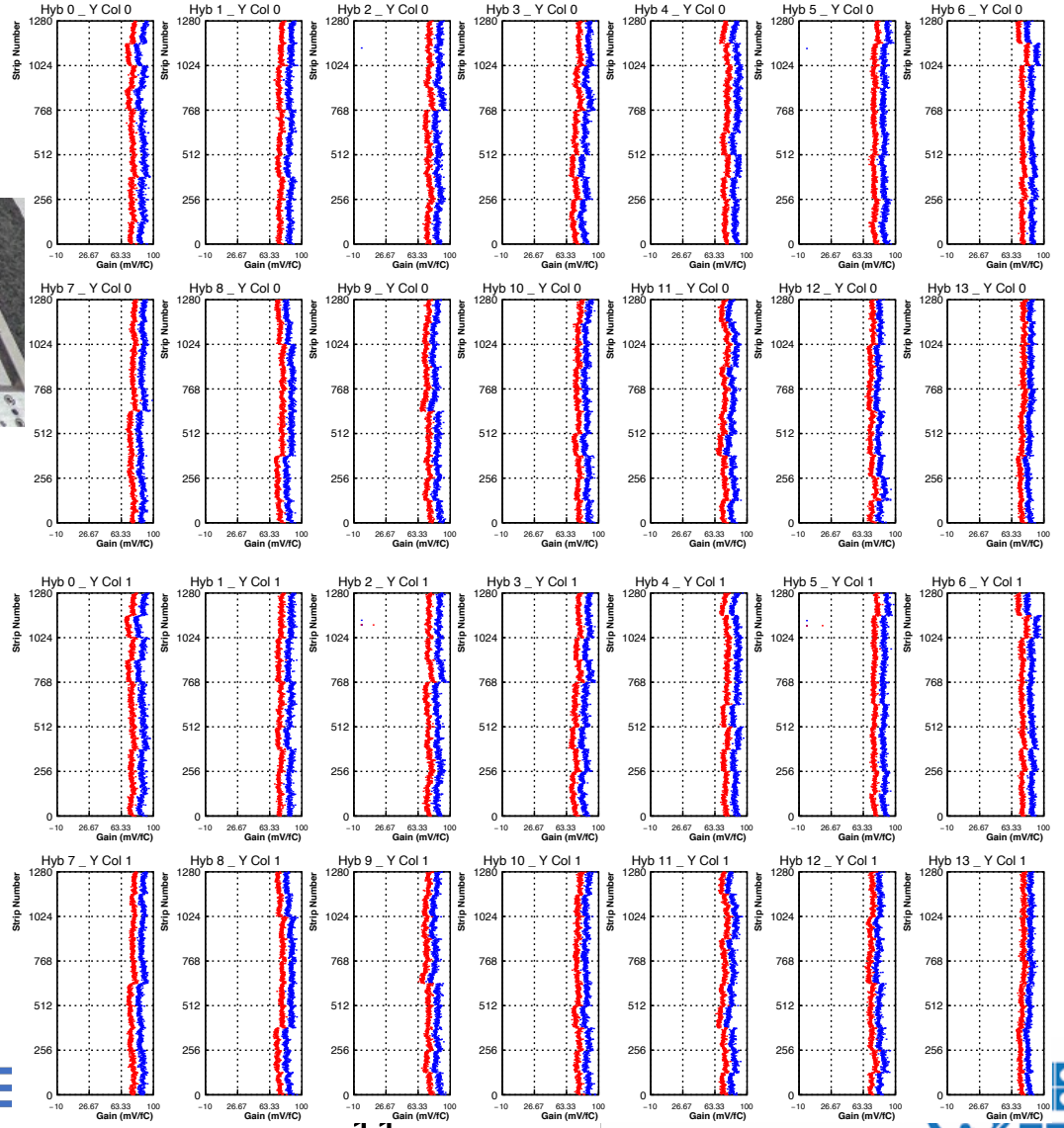

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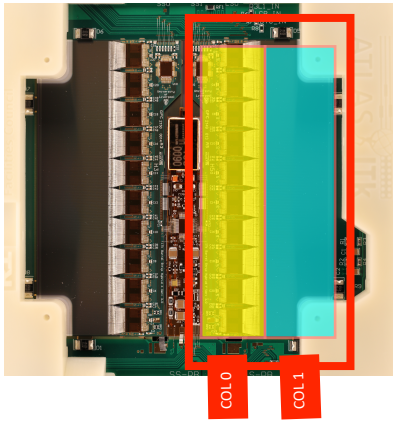

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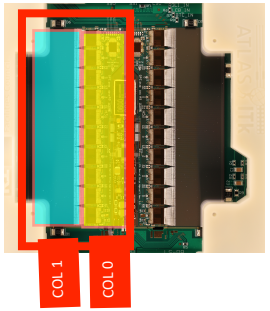
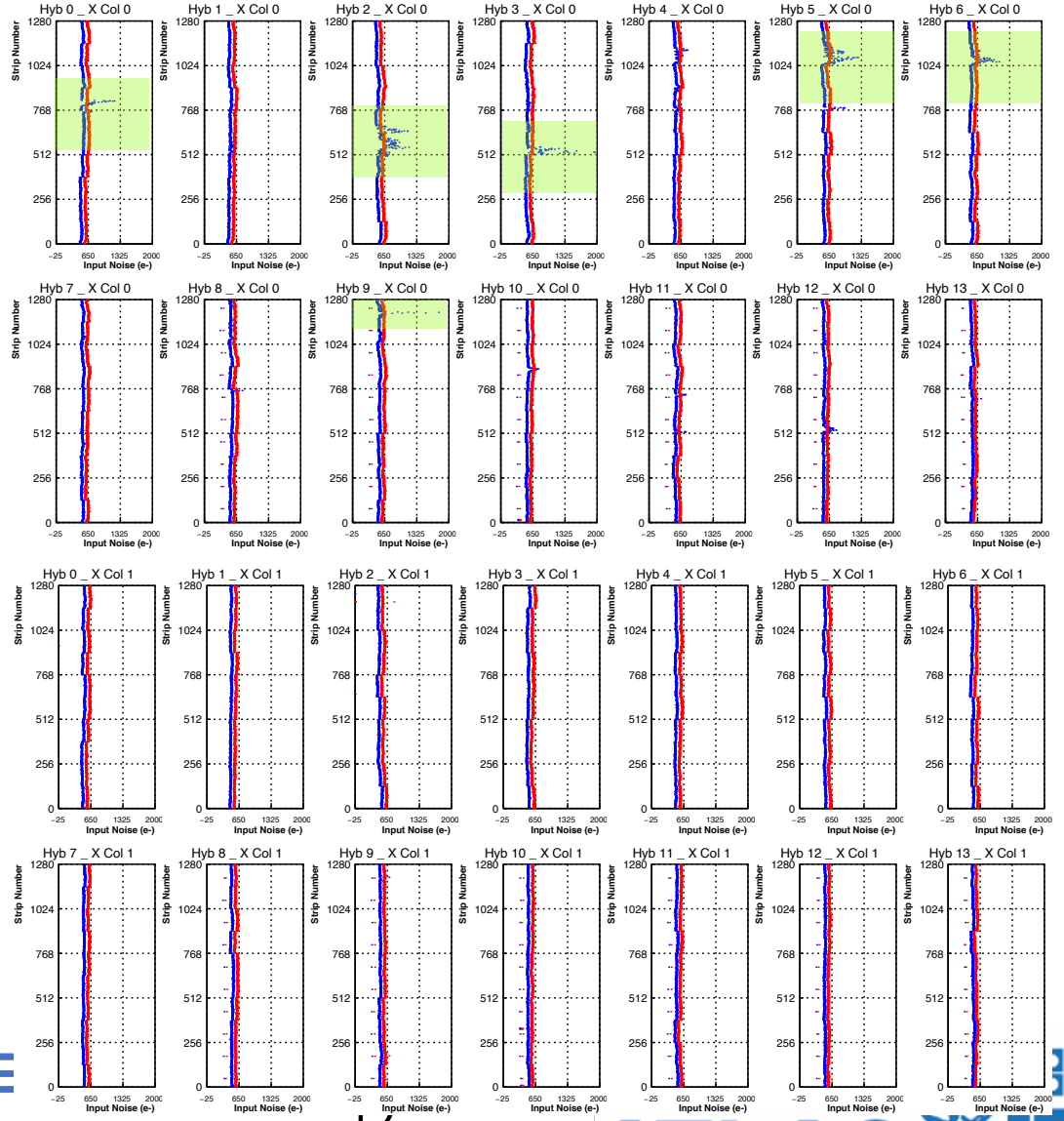


- Input Noise response for the 14 modules on the **MASTER** side
- Input Noise analyzed independently for the two row of strips
- BNL left 1 unbounded channel for ABCStar as investigative tool
- Noise profile good except for Cold Noise issue



- Observed noise peaks at cold temperature (“Cold Noise”) which affect the row of strips which run under the hybrid and the power board

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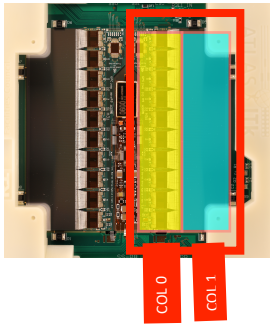

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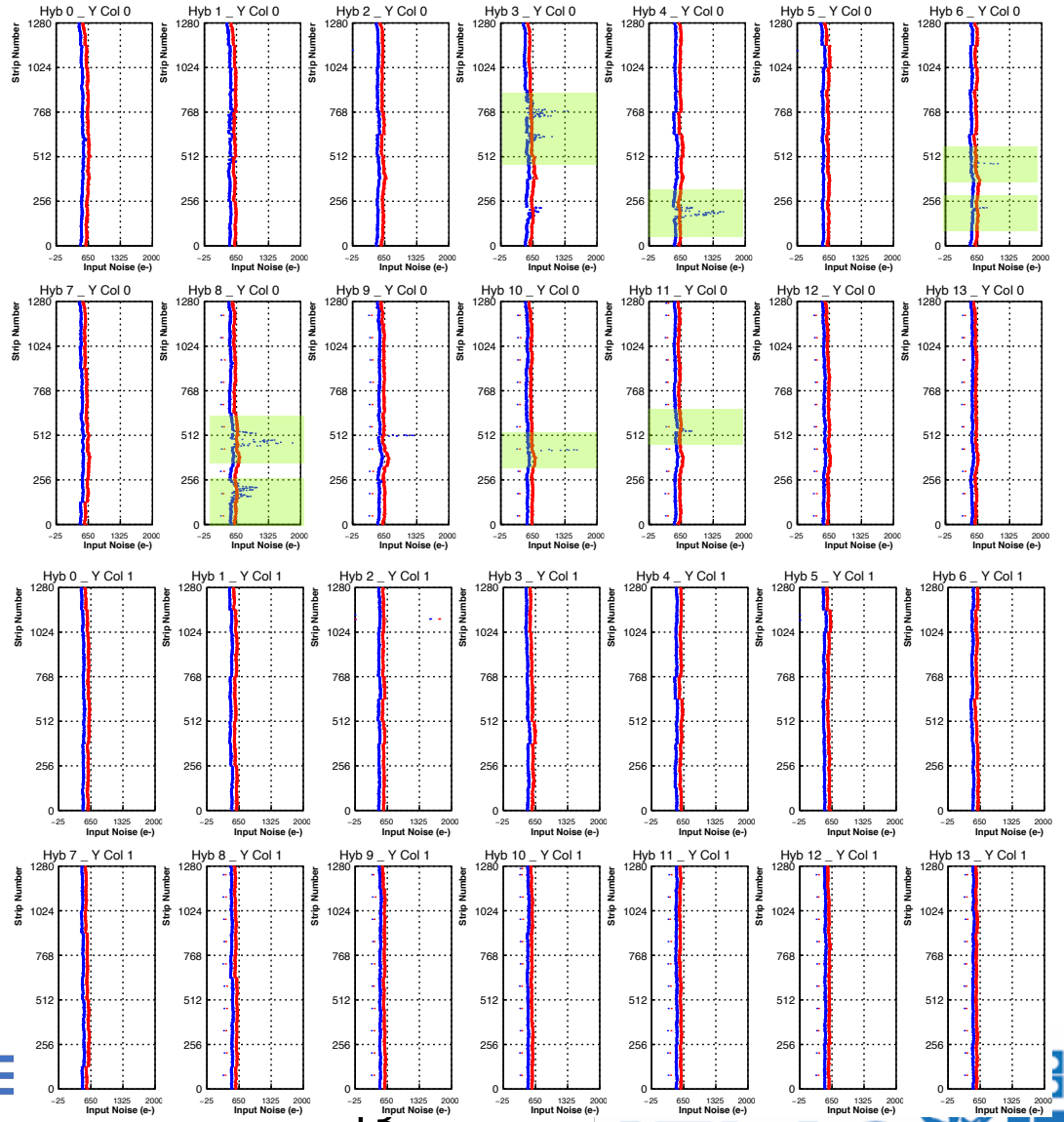


- Observed Cold Noise on row of strips which run under the hybrid and the power board

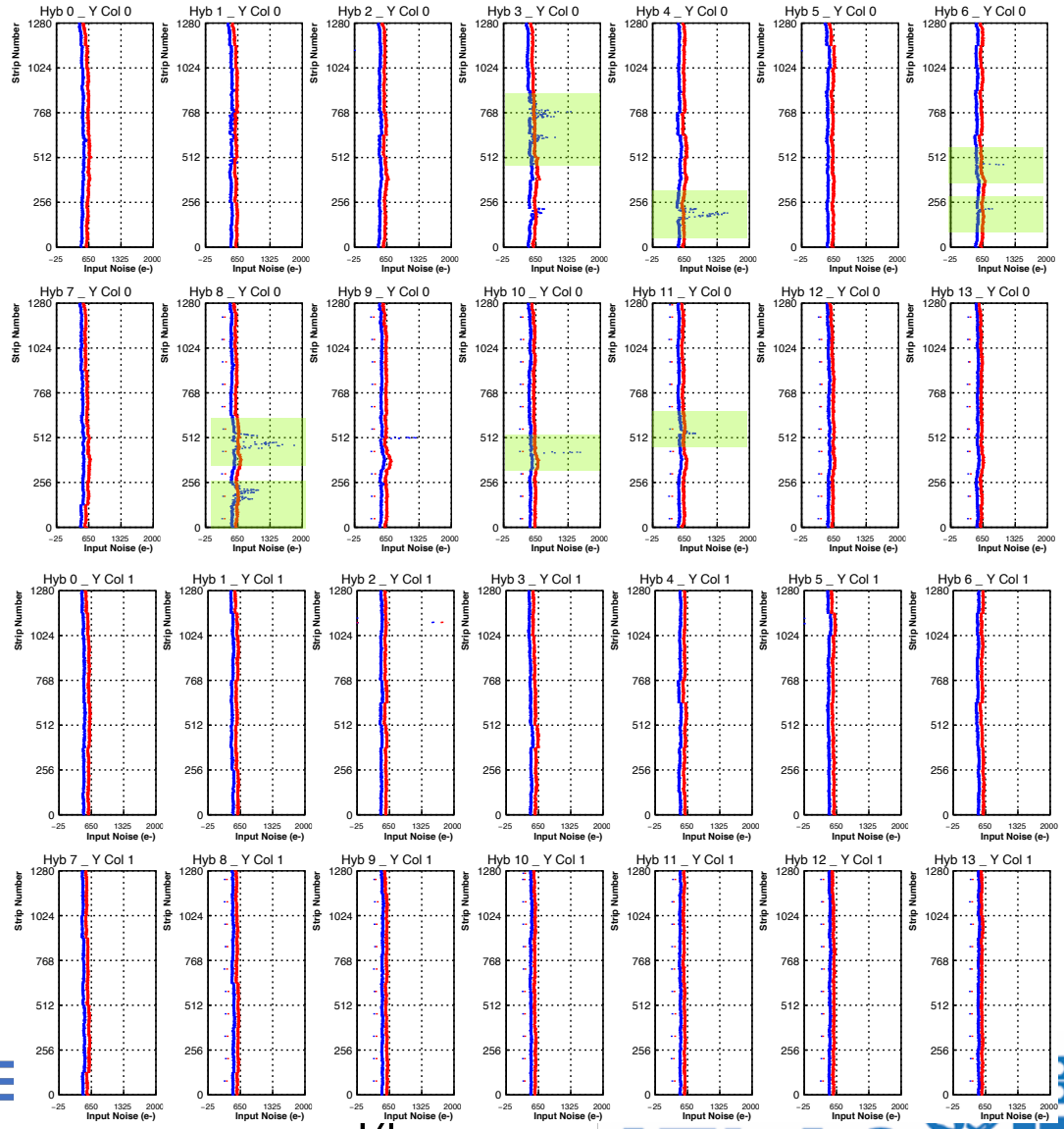
Results Pre-production B stave

T_{inlet} = 24.9 C, -40.5 C

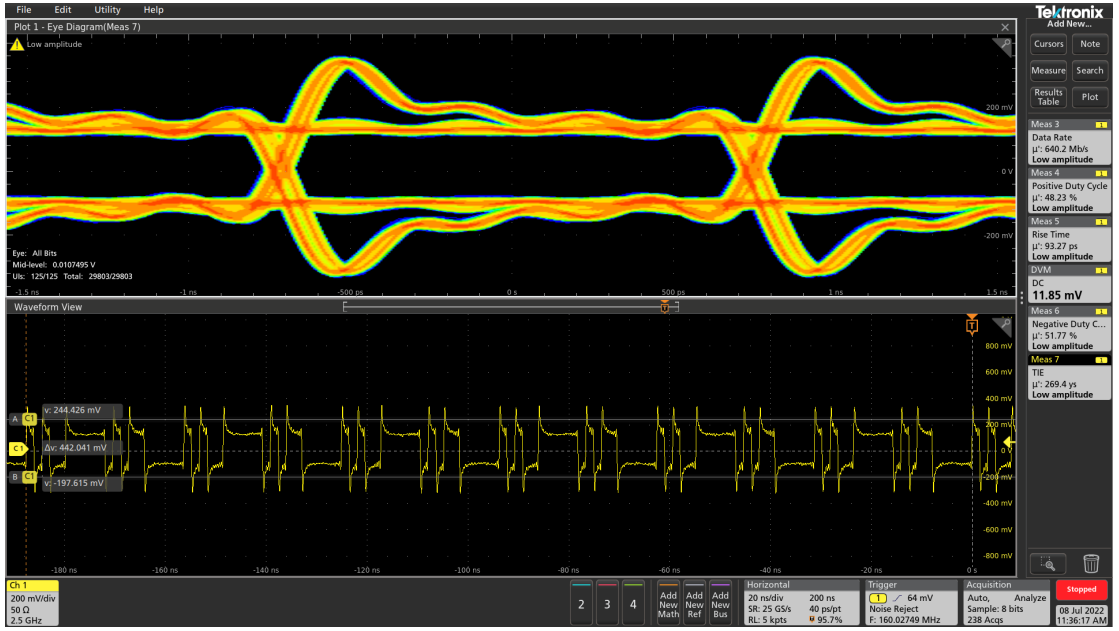
V_{bias} = - 400 V

- Noise peaks have been observed at module level during thermal cycles for both LS and SS modules
- Presence of noise peaks only observed on strips which have the hybrid and power board glued on top
  - Not defined pattern on strip channels affected by noise peaks

- ITk Collaboration has established a Cold Noise Task force to investigate this issue!
  - Lot of progress has been made and will be presented elsewhere

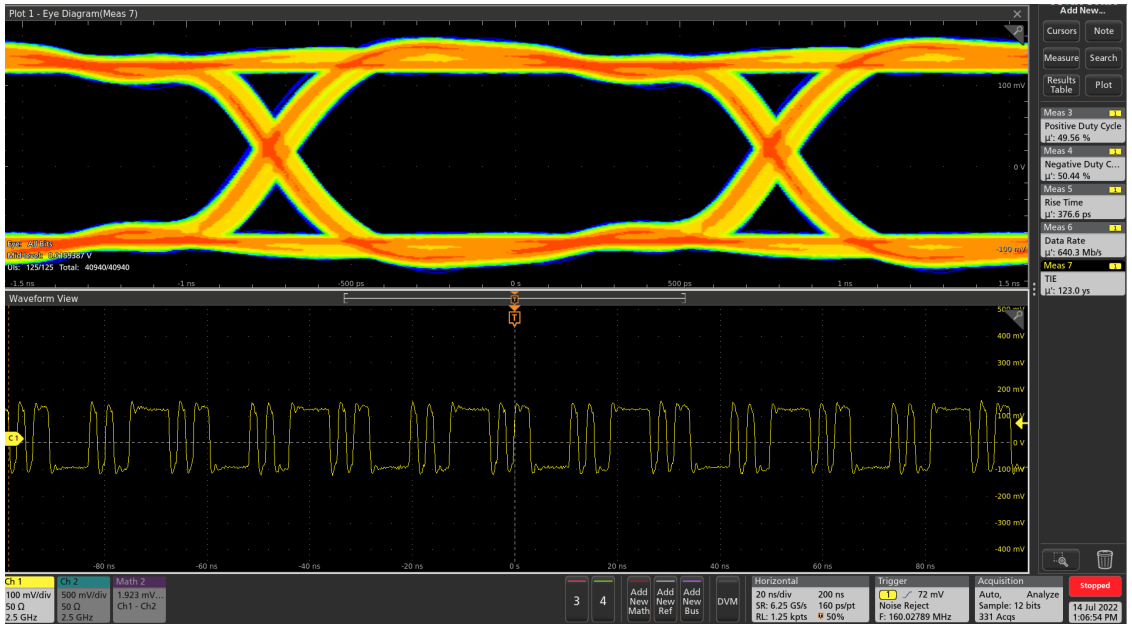


640 Mbit/s Stave signalling



HCC Star 0 Data on Hybrid

DRIVER



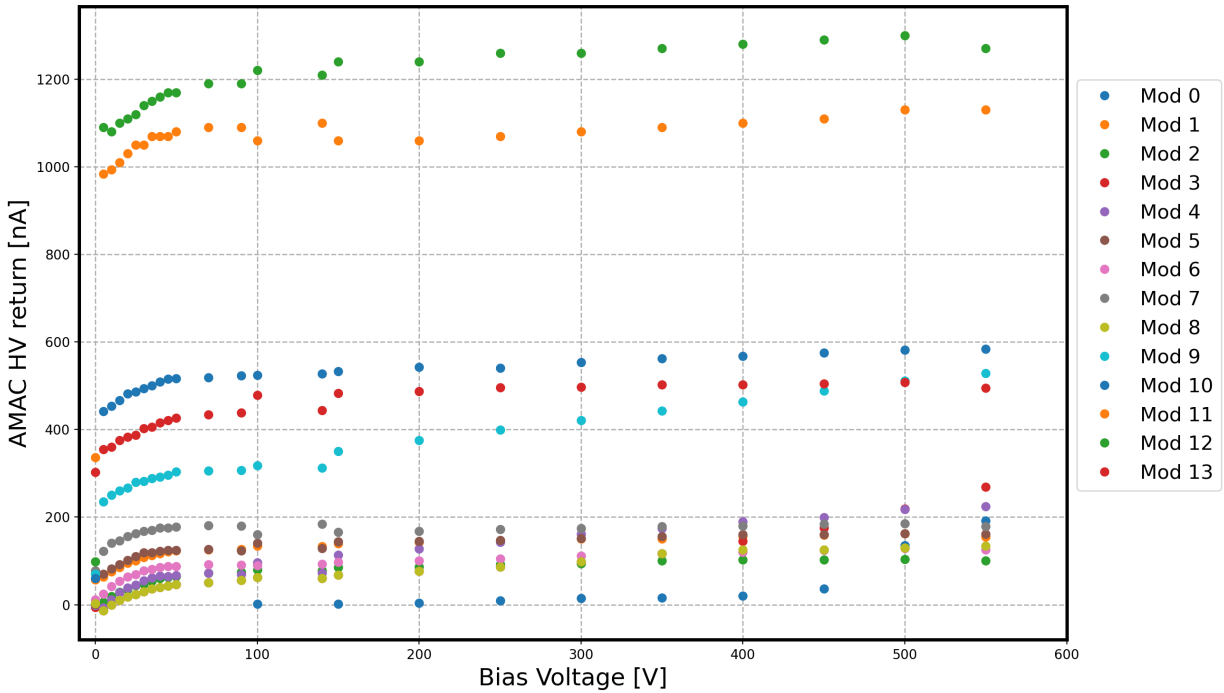
HCC Star 0 Data on EoS

RECEIVER

- As PPB stave is hosting the final version of the HCCStar Chip, the signal integrity at the designed data rate has also been tested
- PPB stave is the first stave we can test 640 Mbit/s data rate:
  - Eye diagrams for HCC Star 0 data transmission at 640 Mbit/s have been measured both on Eos and hybrids
  - No errors observed in BER test at 640 Mbit/s.

AMAC - HV return current measurements

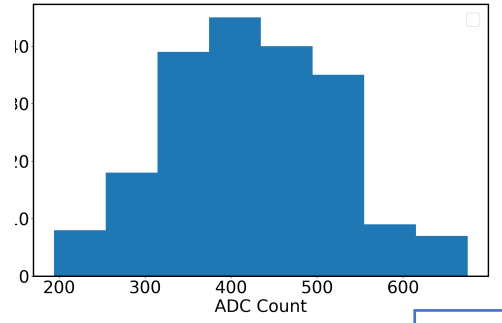
- AMAC provides a mechanism for measuring the HV sensor bias return line
  - Monitoring the leakage current in the silicon sensors become significant during operation, when higher current is expected due to radiation damage
- Current measurement on stave modules are close to expectations
  - Module 11 and 12 are most likely affected by the light from VTRx+
  - Chip-to-chip offset can be corrected by measuring at Vbias =0



- HV return current measurements with prototype AMAC have shown to be deteriorated by noise induced by AC coupling capacitors between HV ret and hybrid ground

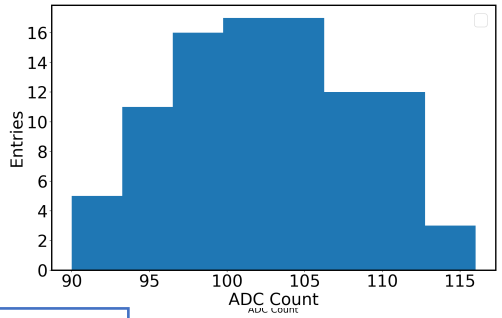
Module on PPA Stave (Prototype AMAC)

Mu = 424.27 ACD Counts , **std = 97.93 ADC Counts**



Module on PPB Stave(AMACStar)

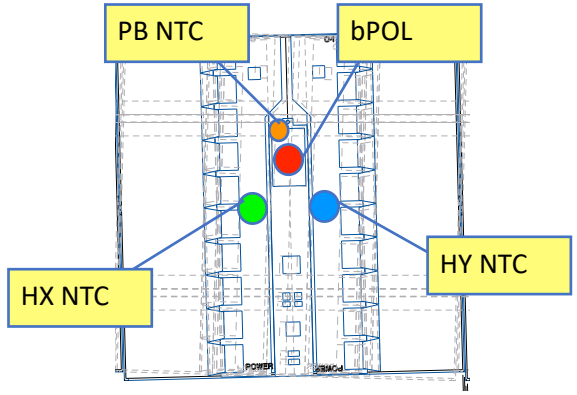
Mu = 102.58 ACD Counts , **std = 5.84 ADC Counts**

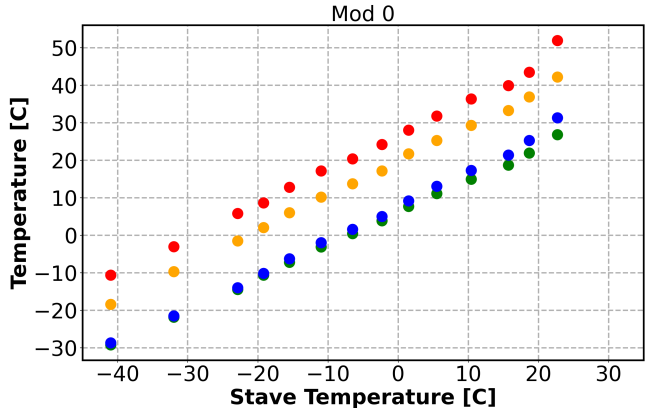


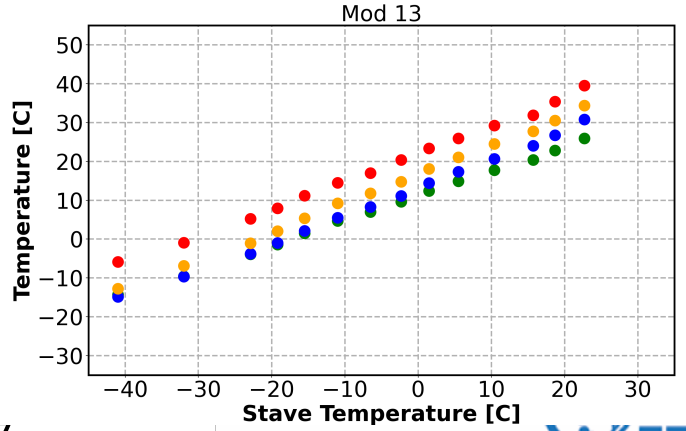
1 ADC Count =~4 nA

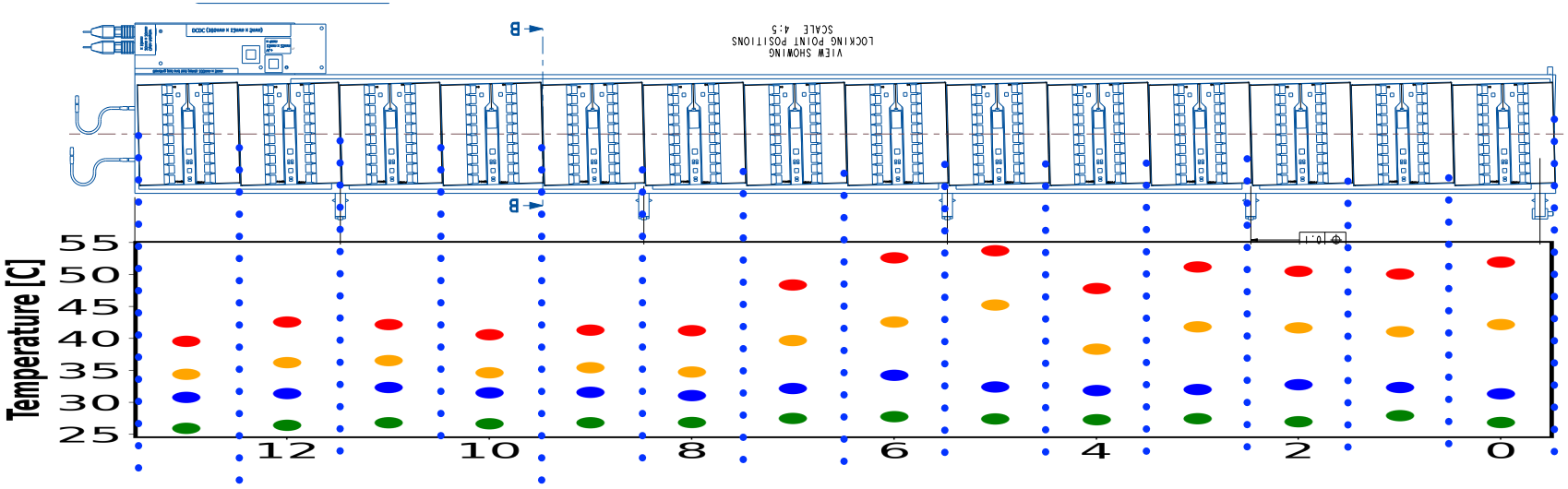
AMAC - Temperature monitoring

- AMAC allows on- stave temperature monitoring using :
  - the 10K NTCs on hybrids and power boards - HX, HY and PB NTCs
  - PTAT channel to estimate bPol temperature
- On-stave temperatures show no obvious trend at Room Temperature
  - Affected by module-module variation
- Module temperatures linear with stave temperature
  - Stave temperature is the average between inlet and outlet temperature
  - bPOL hottest part of Module









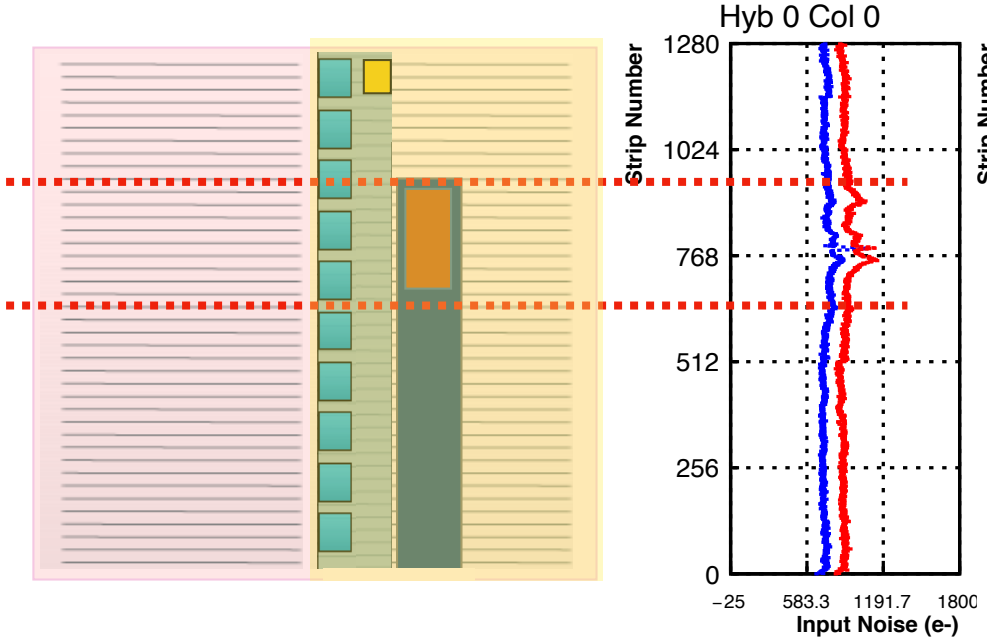
Summary

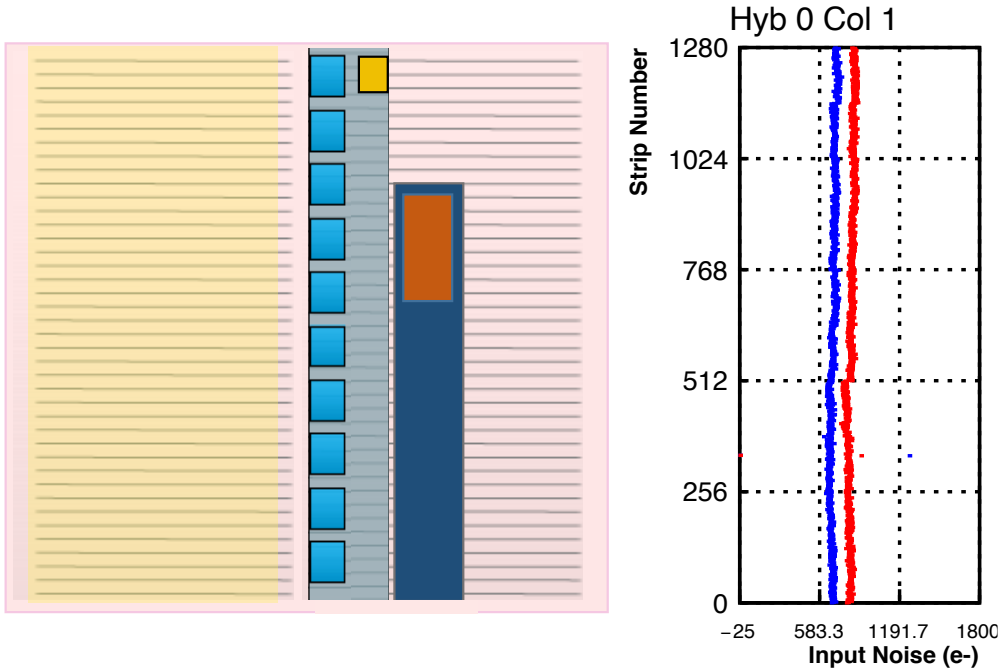
- To cope with larger radiation from the High Luminosity LHC, ITk will replace the current Atlas Inner Detector. The inner layer will be made of silicon pixel detectors while the outer layer will be made of strips detectors.
- The building block of the barrel Strip detector is the stave that houses silicon modules
- Two electrical pre-production staves have been assembled at BNL
- Overall good electrical performance of staves at room and cold temperature.
  Appearance of Cold Noise at cold temperature requires further studies
- Eye diagrams for HCCStar at 640 Mbit/s data rate look reasonable
- Good performance of AMACStar Chip for on-stave monitoring of temperature and current measurements

Electrical performances of pre-production staves for the ATLAS ITk Strip Detector Upgrade

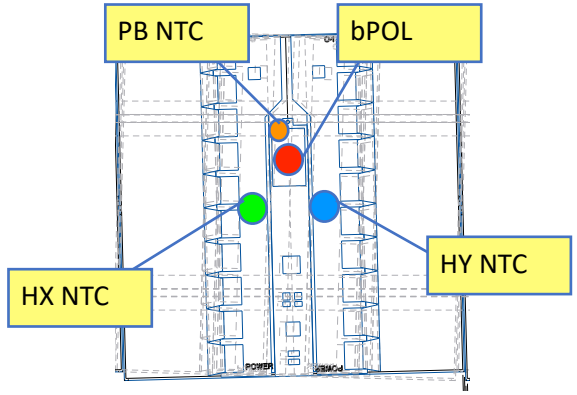
Francesca Capocasa for the ATLAS ITk Strip Collaboration

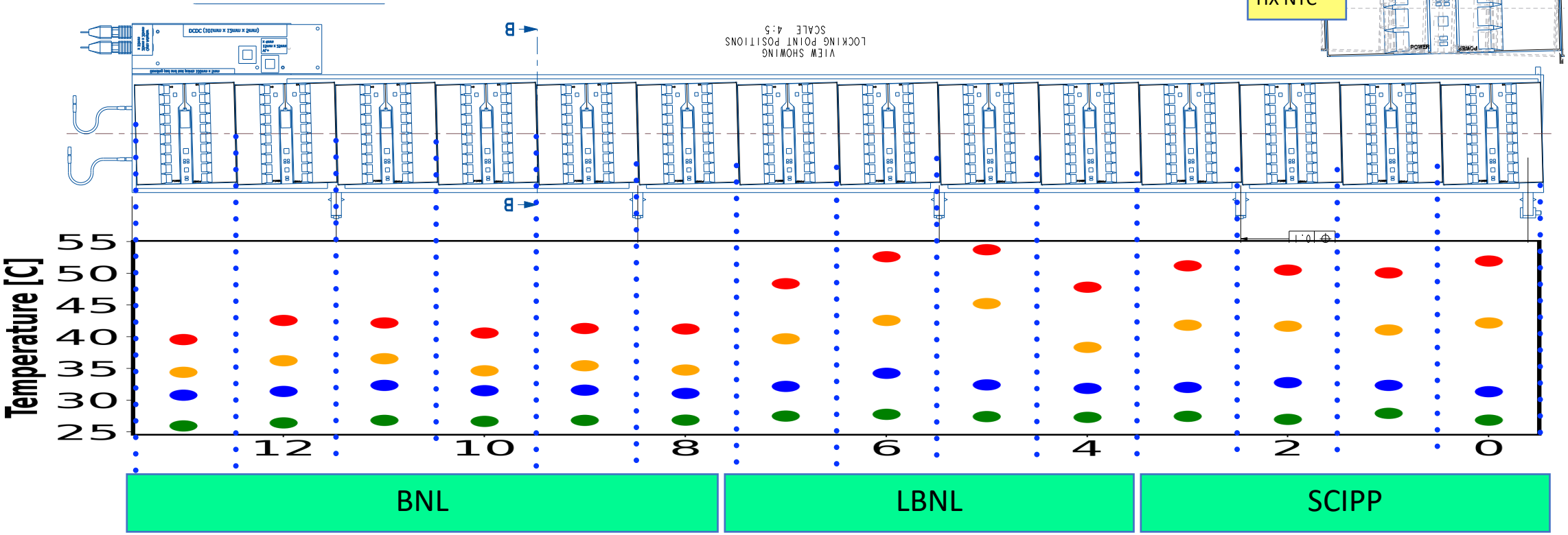
Backup Slides

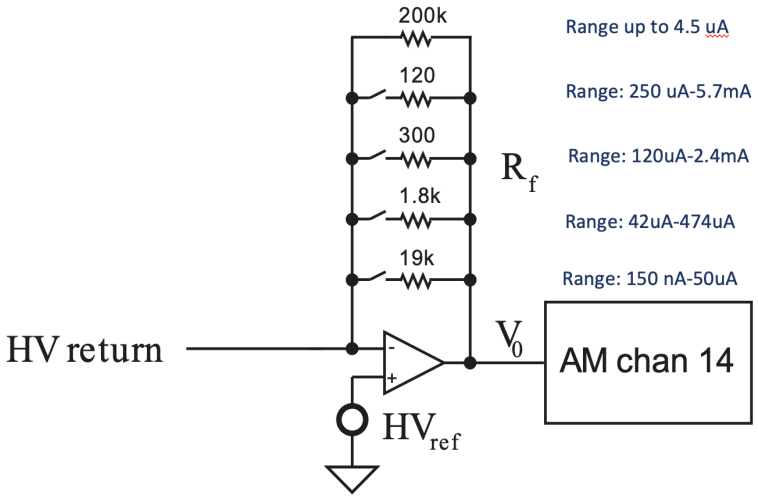

Hyb 0 Col 0
Strip Number
1280
1024
768
512
256
0
−25
583.3
1191.7
1800
Input Noise (e-)

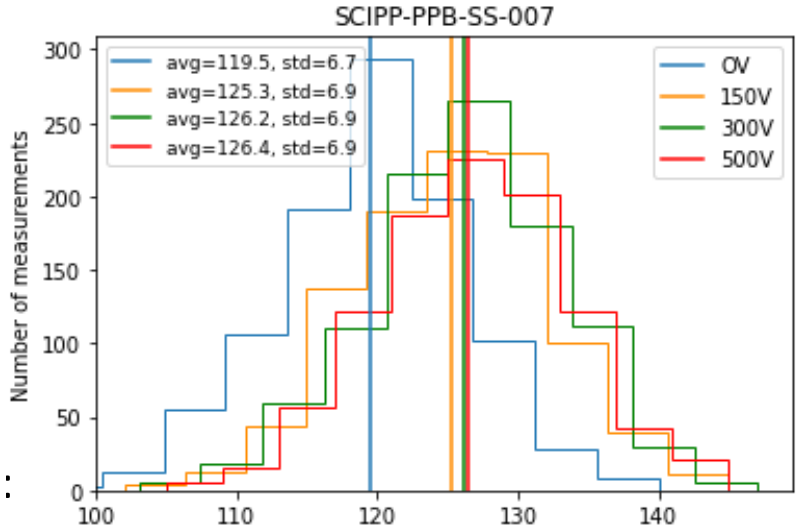

Hyb 0 Col 1
Strip Number
1280
1024
768
512
256
0
−25
583.3
1191.7
1800
Input Noise (e-)

AMAC - Temperature monitoring

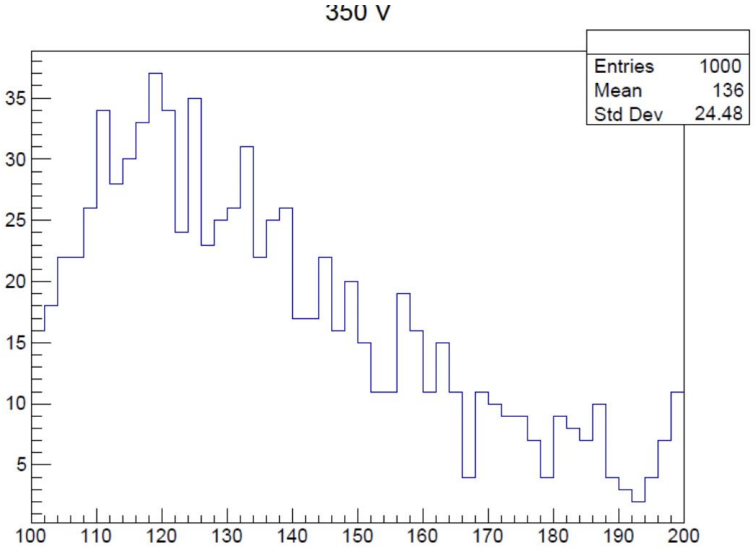


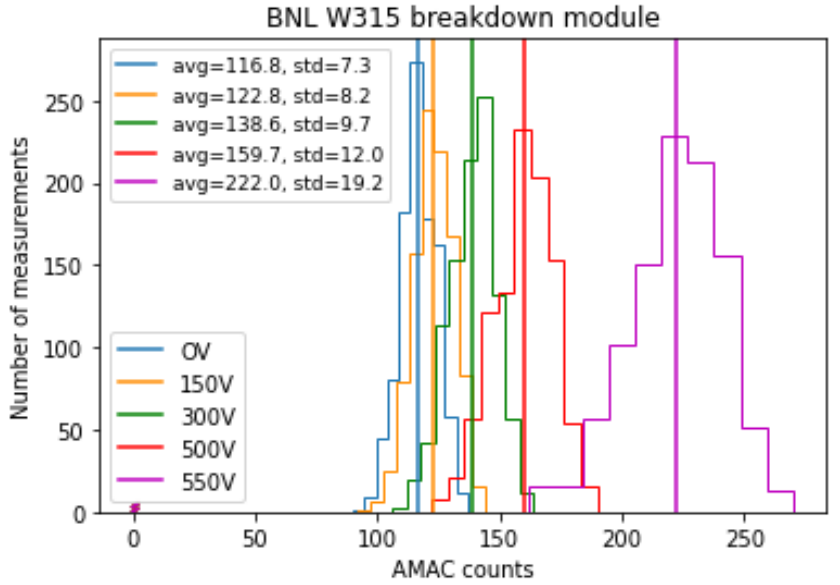



200k
120
300
1.8k
19k
R_f
Range up to 4.5 uA
Range: 250 uA-5.7mA
Range: 120uA-2.4mA
Range: 42uA-474uA
Range: 150 nA-50uA
HV return
V_0
AM chan 14
HV_{ref}


SCIPP-PPB-SS-007
avg=119.5, std=6.7
avg=125.3, std=6.9
avg=126.2, std=6.9
avg=126.4, std=6.9
0V
150V
300V
500V
Number of measurements

AMACv2:


350 V
Entries 1000
Mean 136
Std Dev 24.48


BNL W315 breakdown module
avg=116.8, std=7.3
avg=122.8, std=8.2
avg=138.6, std=9.7
avg=159.7, std=12.0
avg=222.0, std=19.2
0V
150V
300V
500V
550V
Number of measurements
AMAC counts