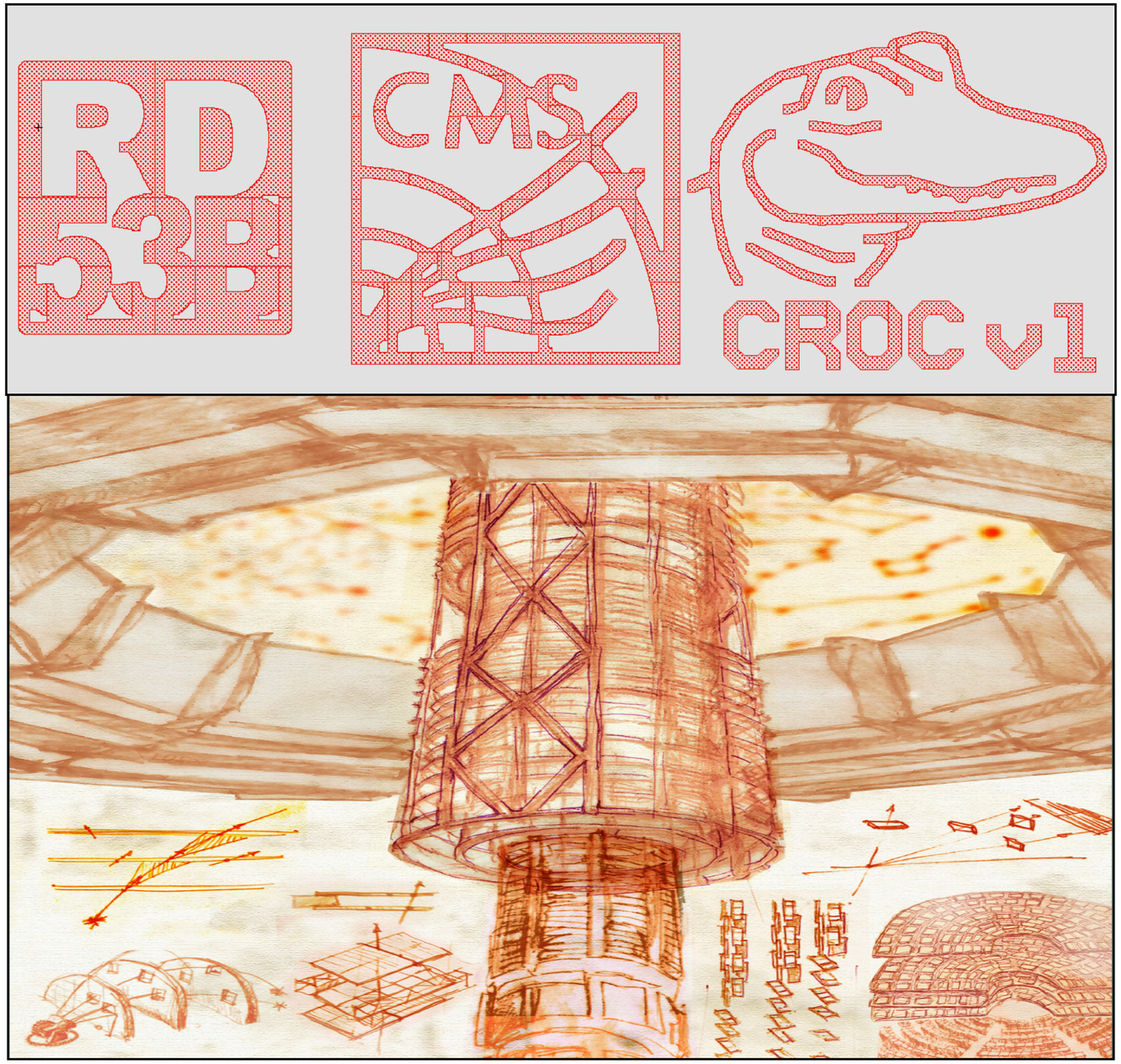

Wafer level testing of CROC

the readout chip of CMS Inner Tracker for HL_LHC - aka RD53B/CMS -

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On behalf of CMS Collaboration

TWEPP 2022, Bergen 19-23 Sept 2022, Norway

Introduction

- The CROC is the CMS version of the RD53 chip.
  - The prototype version is the RD53B/CMS version that followed RD53B/Atlas one, so called ITkPix_v1. The final version will be the RD53C/CMS version that will be basically the identical design with some fixing
- RD53B is a very complex chip: look to this week presentation from Roberto Beccherle :
  - https://indico.cern.ch/event/1127562/contributions/4914053/
- The first proto-CROC wafers arrived in Sept-2021. Chip verification and performance verification started immediately. See posters from Yiannis Kasas and Alkiviadis Papadopoulos
  - https://indico.cern.ch/event/1127562/contributions/4914027/
  - https://indico.cern.ch/event/1127562/contributions/4914028/
- The development of the wafer level testing started in Torino already before CROC arrived
  - previous experience in Torino in wafer testing of RD53A, fully based on hardware and software made by RD53 (Bonn design). We started developing a system based on a CMS based DAQ, writing a new wafer-testing software and extending hardware functionalities.
- Eleven wafers have been tested, for a total of 1518 CROCs.
- This presentation describes the setup/hardw/software, going then through the testing results of the CROC wafers

Purpose of the wafer level testing

Its main goal is to be used during production (pretty obvious but true !)

- **What the wafer level testing SHOULD DO**
  - WLT should **select** well functioning chips
    - during production defects / faults are not at zero level: chip functionality can be affected
    - all functionalities should be tested: all IP-blocks, digital / analog chip functionalities
    - measure digital/analog functionalities according defined quality parameters which can be affected by production variations
    - usage of the chip into the desired application (radiation, potential voltage drops, …) should be considered
  - WLT should **calibrate** those parameters needed for an optimal chip configuration (i.e. module construction) and/or no more accessible later on
  - WLT **testing time** during production should be well compatible with module production schedule
- **What the wafer level testing is NOT designed for**
  - WLT is not meant to make chip characterisation - despite it can give measurements

CROC in a nutshell

- **I/O :**
  - single input line: Clk/Trigg/Com all together; 160 Mbps SLVS receiver
  - four output lines : Aurora lanes; CML tx 1.28 Gbps;
  - input data from a secondary CROC (aka Data merging) : four lanes; SLVS rx 320 Mbps
- **Power:**
  - Analog Chip Bottom: I-DACs, V-DACs, Analog-Buffer, bias distribution
  - Direct powering
  - LDO power mode
  - ShuntLDO
- **Digital** :
  - Digital chip bottom: including 256 global registers
  - Digital pixel array: 2268 COREs each serving (8x8)pixels;
- **Analog Front Ends**
  - 336x432= 145132 Linear Front Ends
- **Monitoring**:
  - ADC
  - Sensors: Temperature; Radiation; Ring Oscillators;

Probe card

WPAC (Arduino) ⟷ I2C (CMOS I/O, Multiplexer)

V_{out} ← Ext-Multimeter

Analog Multiplexer on probe card to allow measurements of many voltages monitored by CROC VMUX and sensing chip additional voltages/GNDs

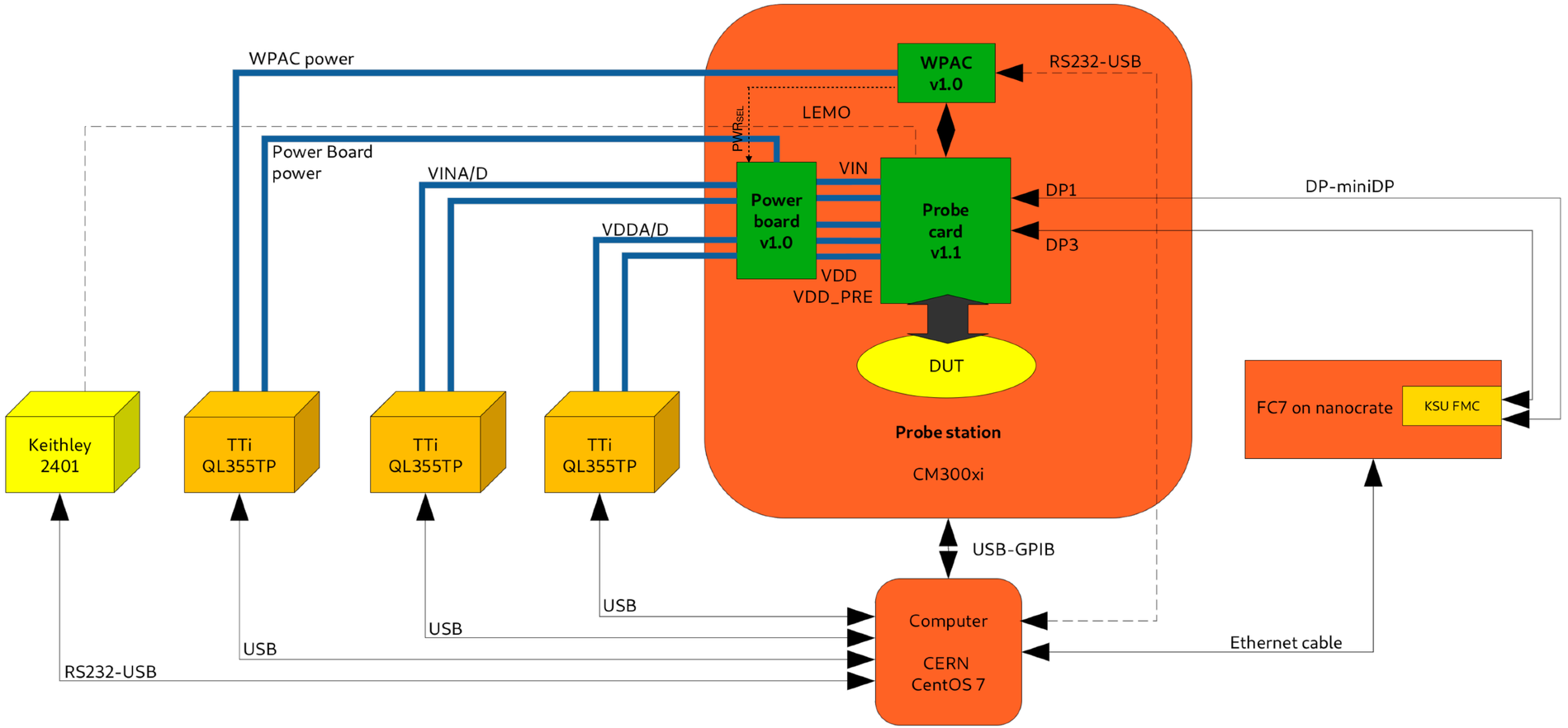
$V_{PLL/CML}$ $V_{INA/D}$ $V_{DDA/D}$ V_{DDpre} — I/O — Data Merging — LVDS Output for Monitoring

Power Board — from FPGA / FC7

Development of new probe-card: starting from base design of RD53B used for Atlas submission:

1. I2C control of IC of the probe-card via Arduino mounted on WPAC-board (not only FPGA)
2. All Powering schemes possibles: included also direct power - use of power board
3. Possible to use Keithley or WPAC for ADC-calibration or Voltage measurement
4. Additional features added (i.e. different ShuntLDO slope, direct power)
5. More compact design to allow WPAC and probe-card placed in the probe-station

Hardware architecture

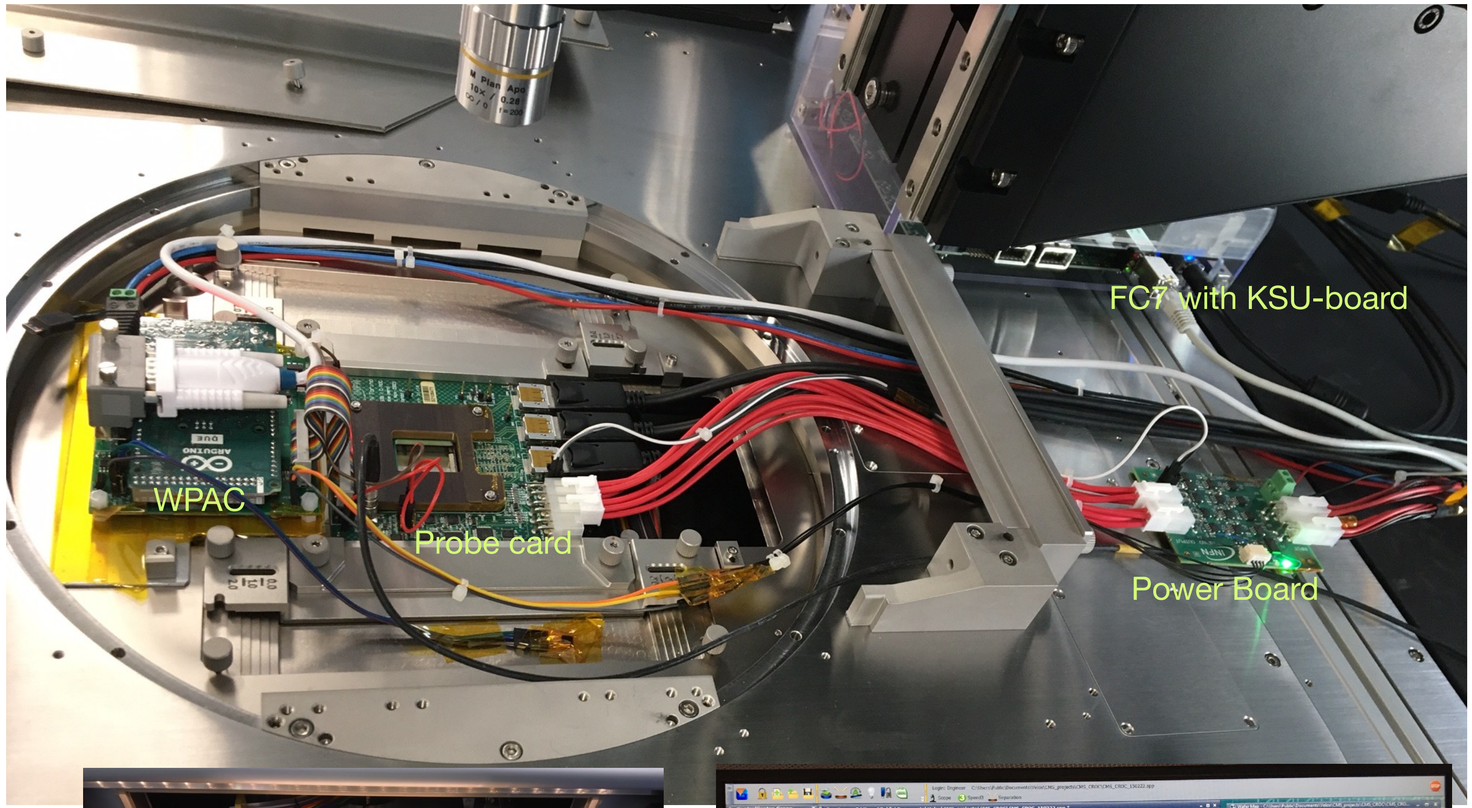


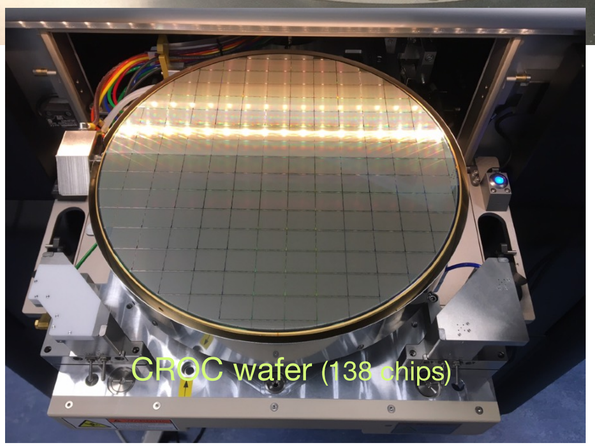
- Probe station: Cascade Microtech CM300xi semi-automatic probe station;
- CROC probe card;
- DAQ board: FC7 with KSU FMC;
- Wafer Probing Auxiliary Card (WPAC) with mounted Arduino Due board;
- Power supplies: TTi QL355TP;
- Source-meter unit: Keithley 2400/1 Controlling computer

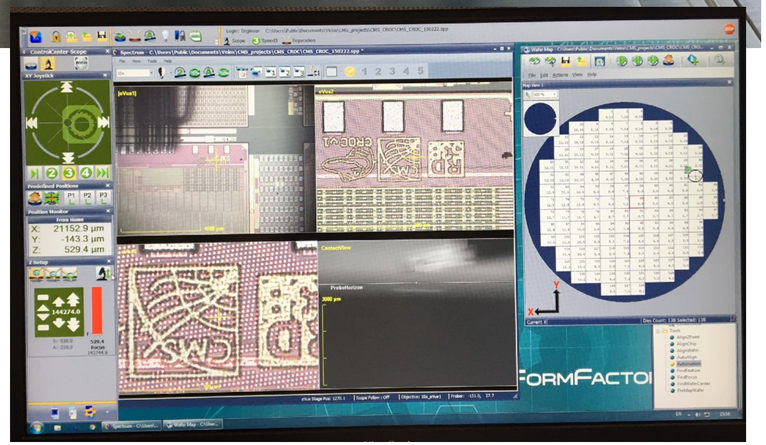
https://gitlab.cern.ch/croc_testing/croc_wlt/-/wikis/Hardware-setup

Wafer Probing setup@Torino

Wafer Probing setup@TORINO

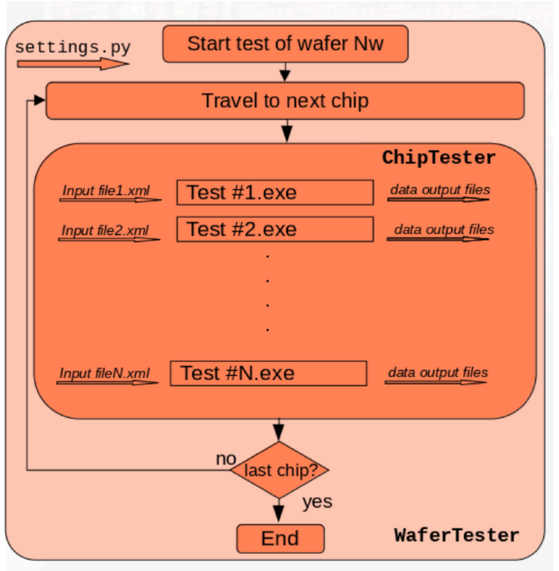




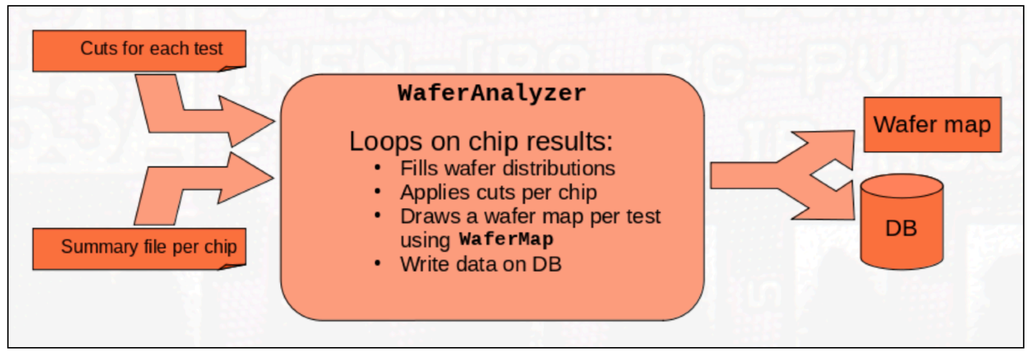


The software setup for CROC wafer-level testing consists in:

- Operating system: CERN CentOS 7;
- Python 3.7;
- GPIB library for controlling the probe station;
- **croc_wlt** wafer-level testing package, which contains:
  - modules for chip testing and probe station control;
  - modules for data analysis;
  - library for interfacing with the probe station via GPIB;
  - library for sending commands to the WPAC;
  - library for controlling the power supplies and source-meter unit.



- Repository: https://gitlab.cern.ch/croc_testing/croc_wlt
- Documentation: https://gitlab.cern.ch/croc_testing/croc_wlt/-/wikis/home



Testing Procedure

LDO testing

1. Startup in LDO
2. IREF trimming
3. Communication
4. Writing of efuses
5. VDD trimming
6. Global registers ▽
7. Injection capacitance measurement
8. ADC calibration
9. DACs calibration
10. Ring oscillators calibration
11. Temperature sensors calibration
12. Chip bottom and matrix power consumption
13. LDO *IV* curve

SLDO testing

14. Startup in SLDO
15. SLDO *IV* curve (+ OVP)
16. Aurora lanes ▽
17. Chip ID ▽
18. Pixel registers ▽
19. Data merging ▽
20. Digital scan ▽
21. Analog scan ▽
22. Threshold scan (coarse) ▽
23. Threshold tuning ▽
24. Threshold scan (fine) ▽

Work-on-going: **Scan-Chain test**

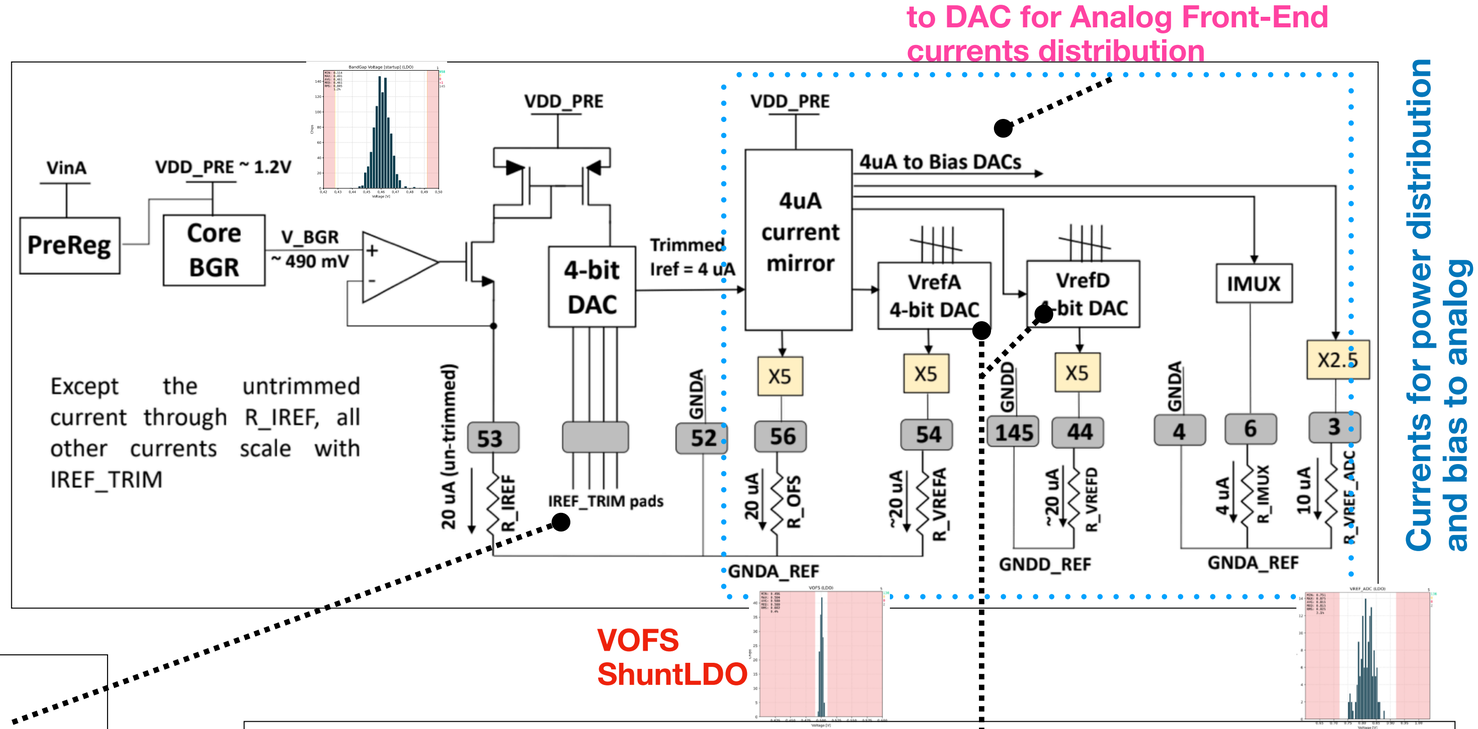
- power
- trimming
- I/O
- digital test
- calibration
- analog test

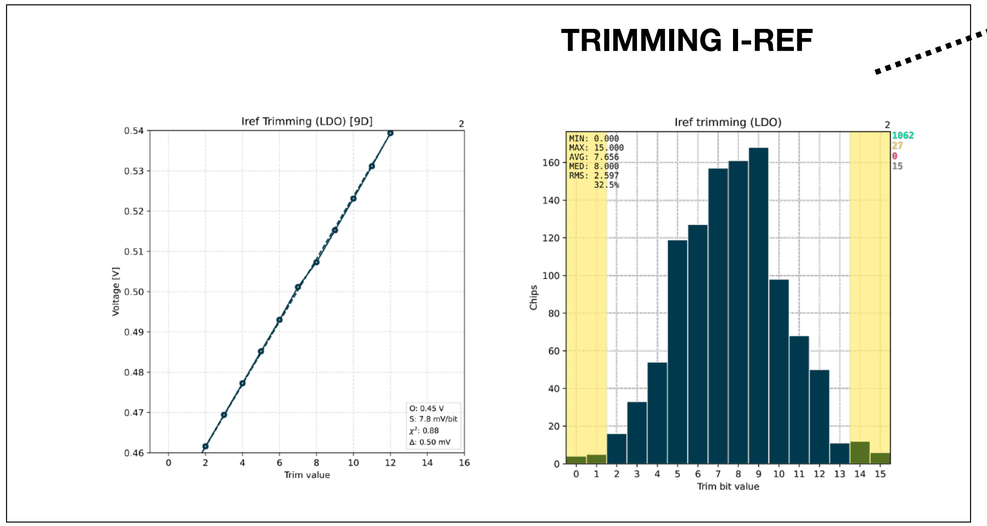
▽ test done with VDDD=1.1V

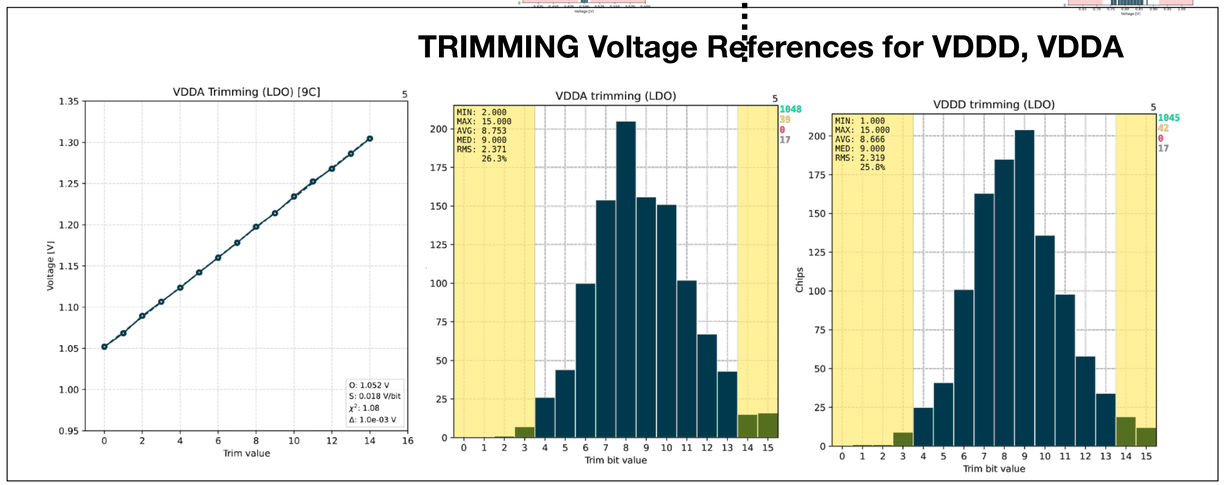
CROC Trimming(s)

Starting from a preregulator and a BandGap, in order to get **calibrated** Voltage and currents distribution a double trimming is needed

1. Trimming of current reference (from ext-pad)
    1. defines chip **wire-bonding** at module construction
2. Trimming of VDDD, VDDA (from configuration registers)

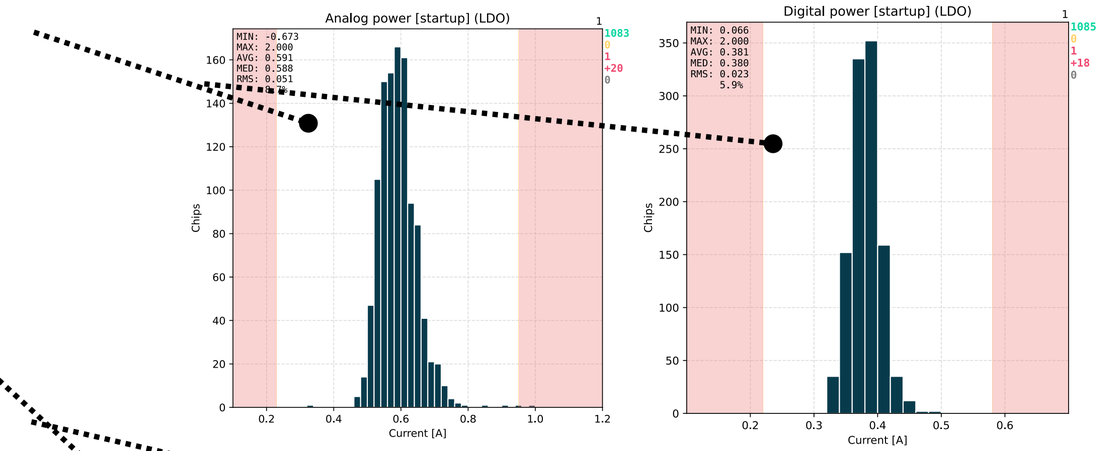


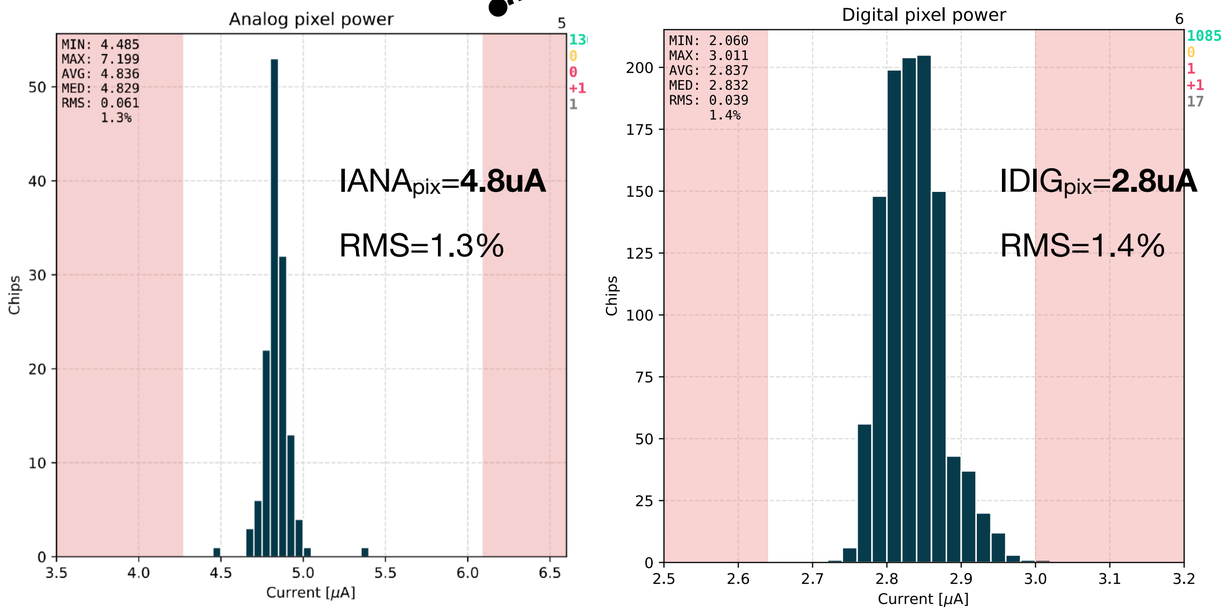


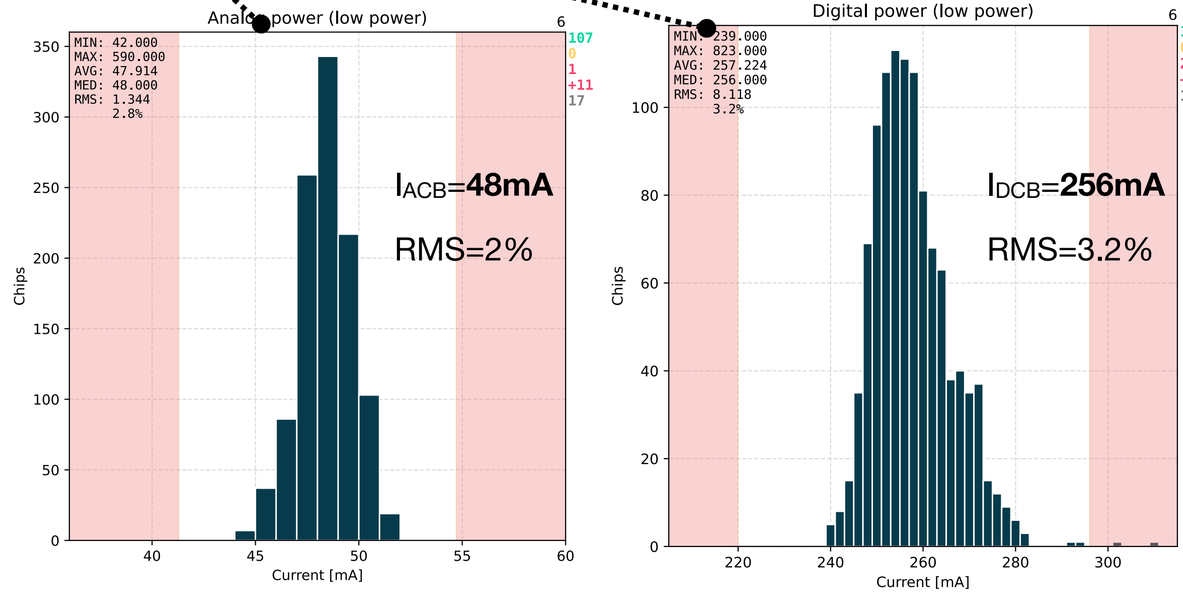


CROC Power

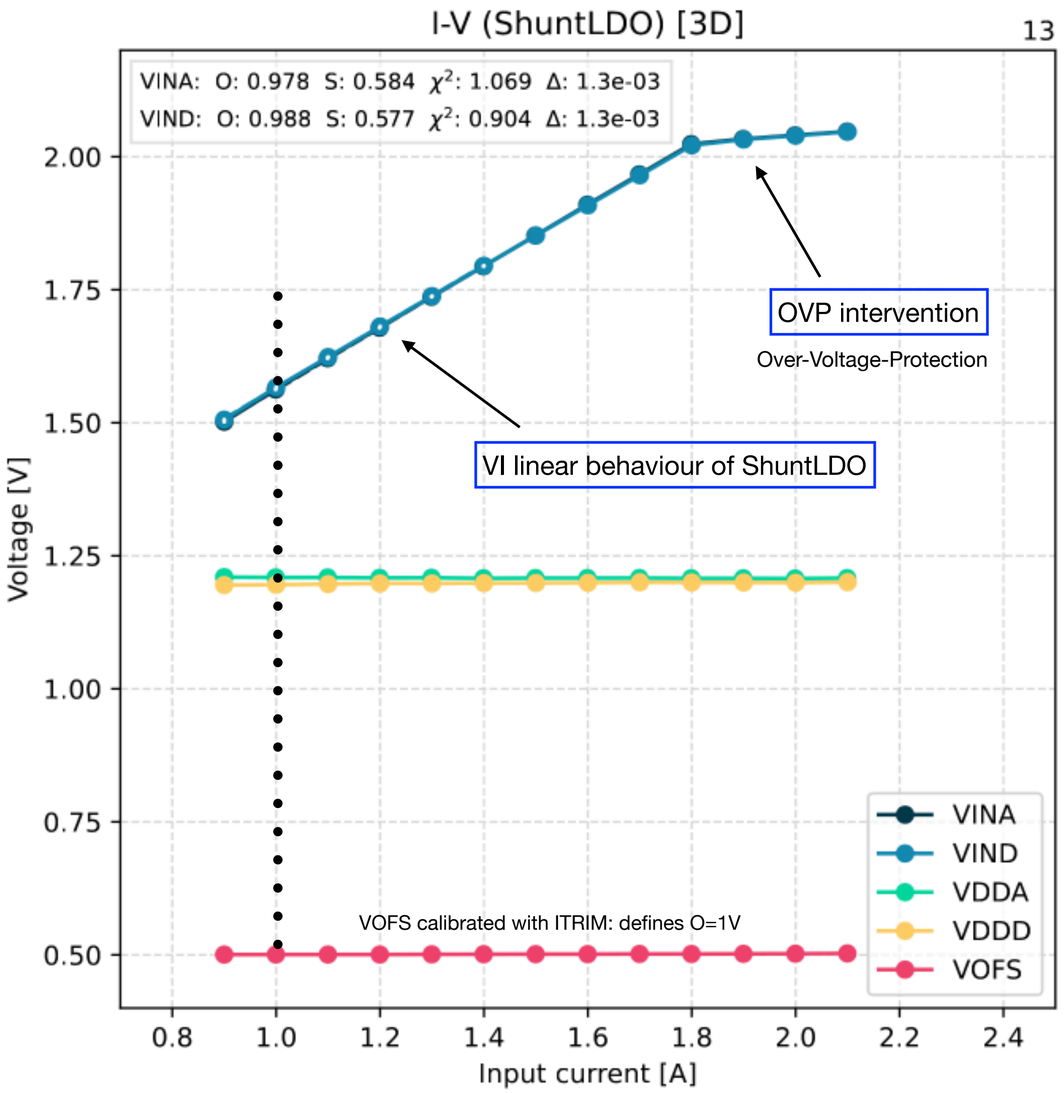
- Anomalous currents - low/high before any trimming
- Current by chip bottom : Analog (ACB) / Digital (DCB)
- Current taken by pixel (averaged into the matrix)
  - verification of pixel power consumption
- IV of Shunt LDO (see next slide)



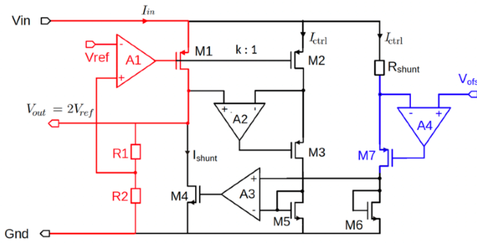




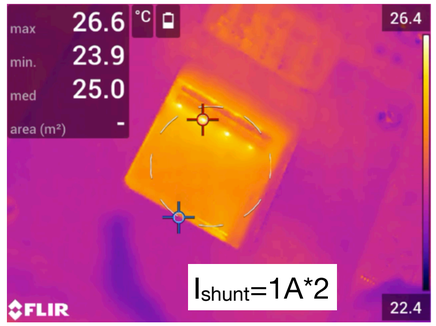
ShuntLDO IV

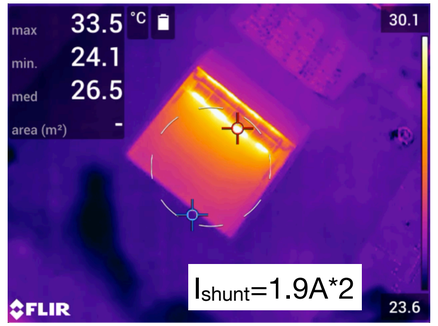


- Fundamental for serial powering of modules: fixed current provide power to CROC, statisfies its consumption request - regardless to current variation - and remaining current goes to a shunt resistor

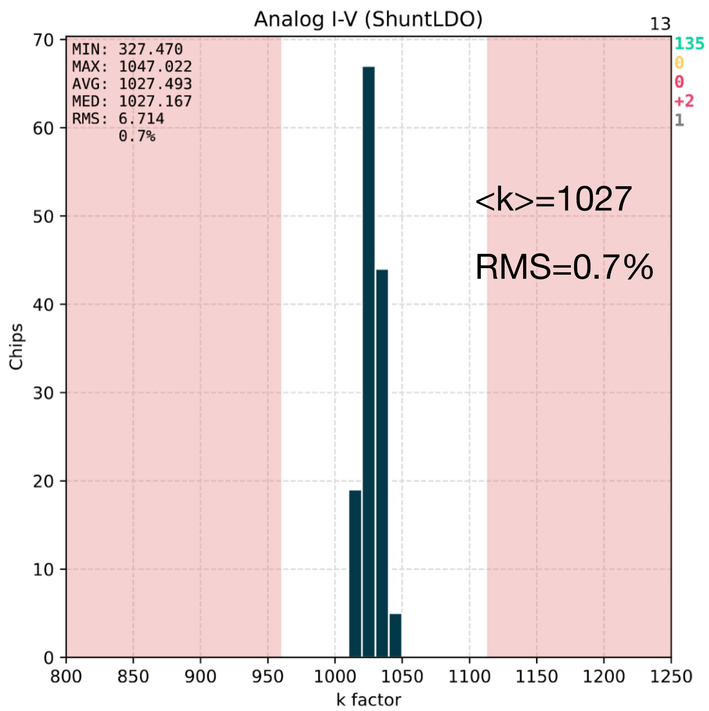


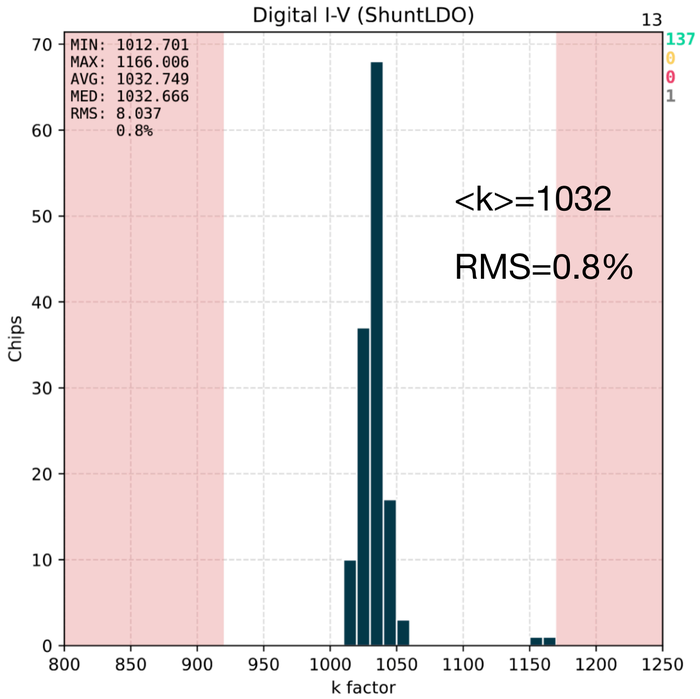
- NB: the current is x-axis is for a single power domain, analog and digital are independent here. This allow to characterise each ShuntLDO
- Chip is configured to operation values, therefore 800mA goes to ACB+Matrix(ana) and 668mA goes to DCB+Matrix(dig)
- Rshunt=597,35 Ohm; S=Reff=0,584Ohm k=1022
- The over voltage at ~2V is reached at ~1.8A
- All other tests done in ShuntLDO are done at I=1A, therefore 2A total

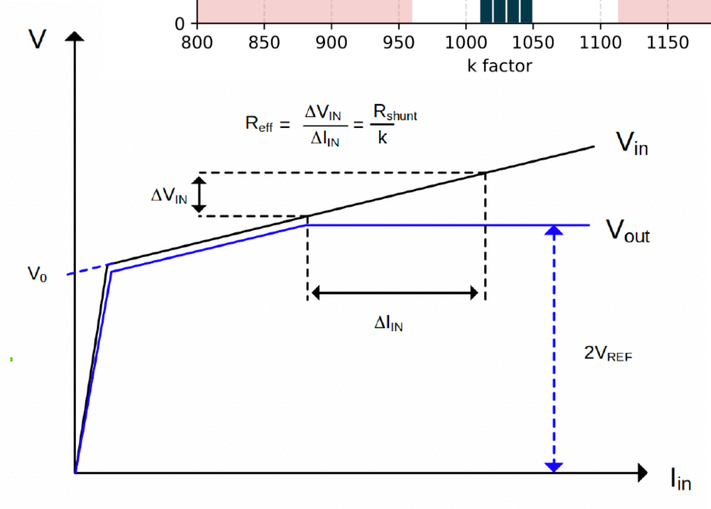




ShuntLDO IV

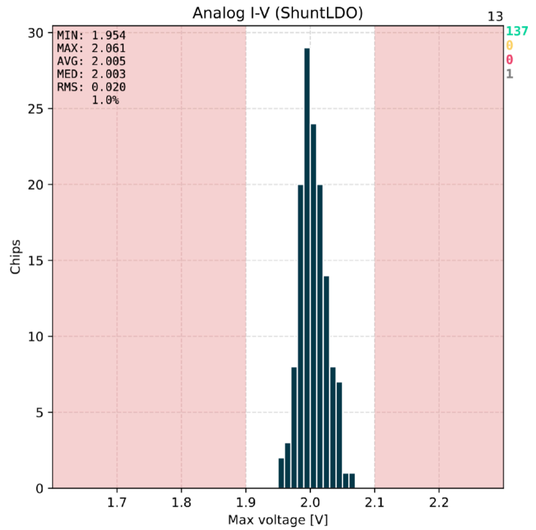


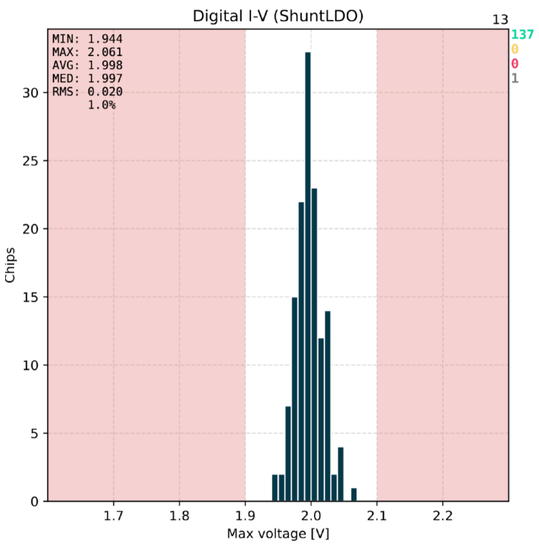




k-factor and Offset measured by fitting IV

Overvoltage protection working well …





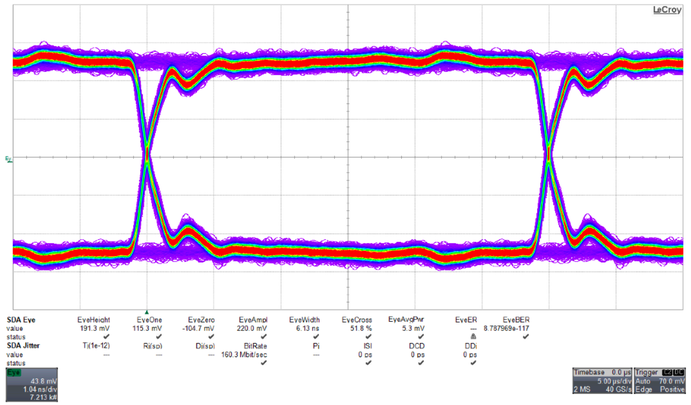
I/O and Digital tests

I/O Communication

input signal at minimum differential amplitude : check of **SIvs-rx, CMD**, **PLL**

output verified with all four lanes: checks **CML**

tried also for different ChipIID (different identifier for chip sharing same input line)



Data merging

FPGA sends data patterns, acting as a secondary chip. DUT is verified to work as primary chip

Global register test

test all Global Register (located on periphery) : vectors 0b0101010101010101; 0b1010101010101010 ;

verify Write&Read for ~150 registers

Pixel register test

test all Pixel Register (located on pix-matrix) : vectors for two pixels 0b0101010101010101; 0b1010101010101010

verify Write&Read for ~ 145132 8b-registers

Digital Scan

test the digital from end of the chip, injecting digital signals for each pixel, therefore it uses all the digital COREs of the chip (8x8) px

Scan-chain :

A scan chain is an industrial standard technique used in design for testing. The objective is to make testing easier by providing a simple way to set and observe every Flip-Flop in the Integrated Circuit

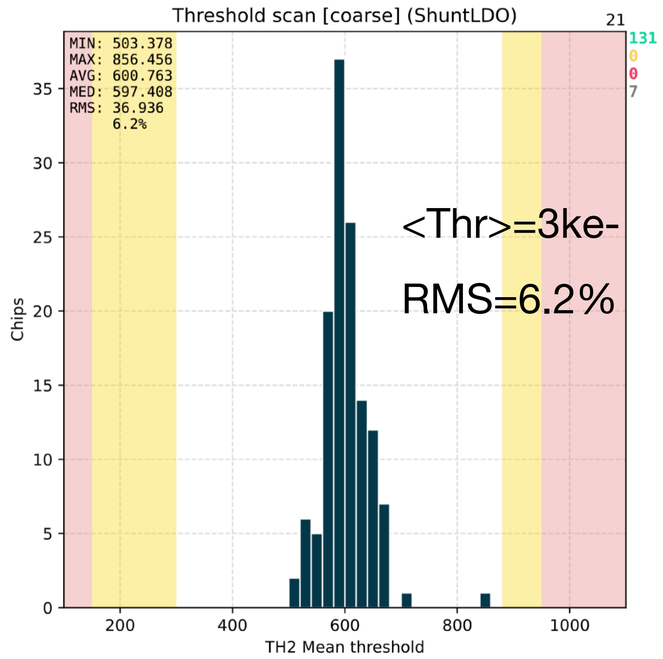
Development from the CMS-DAQ side is now under implementation for wafer testing to make it fast and usable in the setup

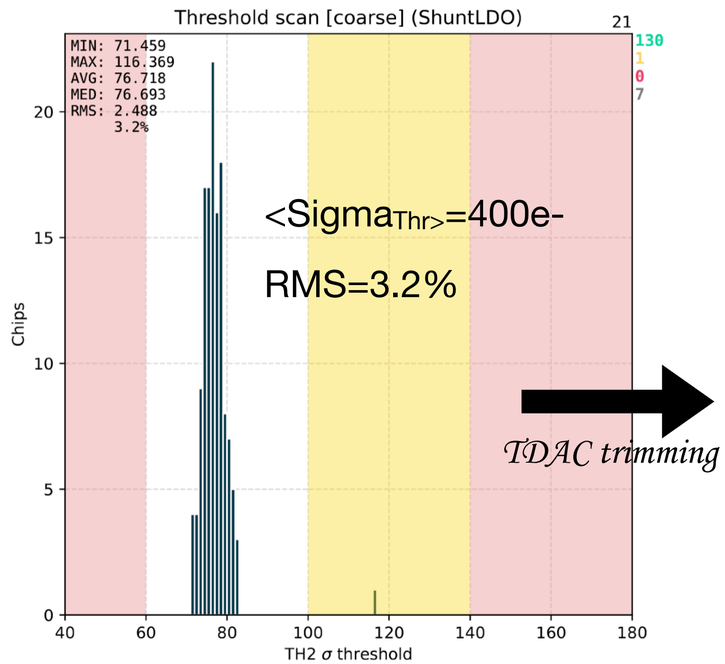
with 2023 vector, each with 312111 bit, almost the 99.9% of the CROC periphery is verified in a time of ~40-80”.

Analog tests

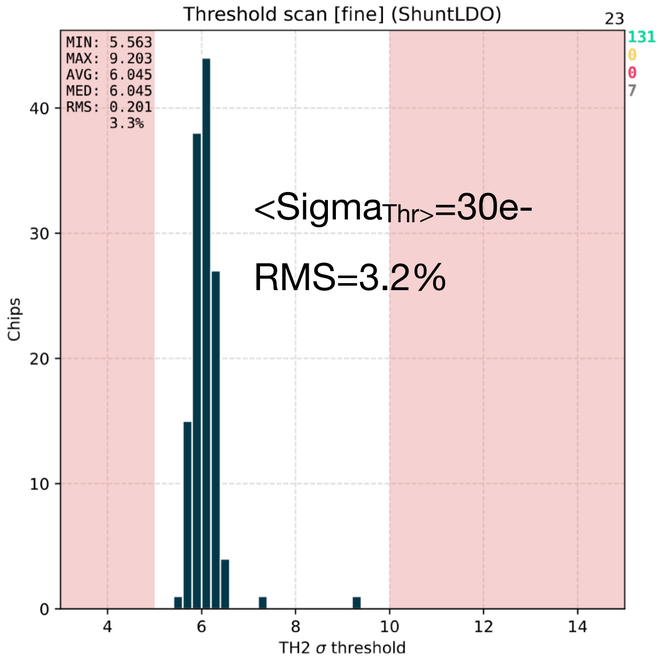
Several tests sending a stimulus to **Analog Front Ends**, via charge injection

- **Analog scan:** check 100% efficiency for high signal
- **Analog threshold scan** : S-curve measurement to measure threshold
- **Threshold trimming :** threshold equalisation per pixel - verifies Trimming DAC (TDAC)
- **Analog trimmed threshold scan:** verifies for all pixels that

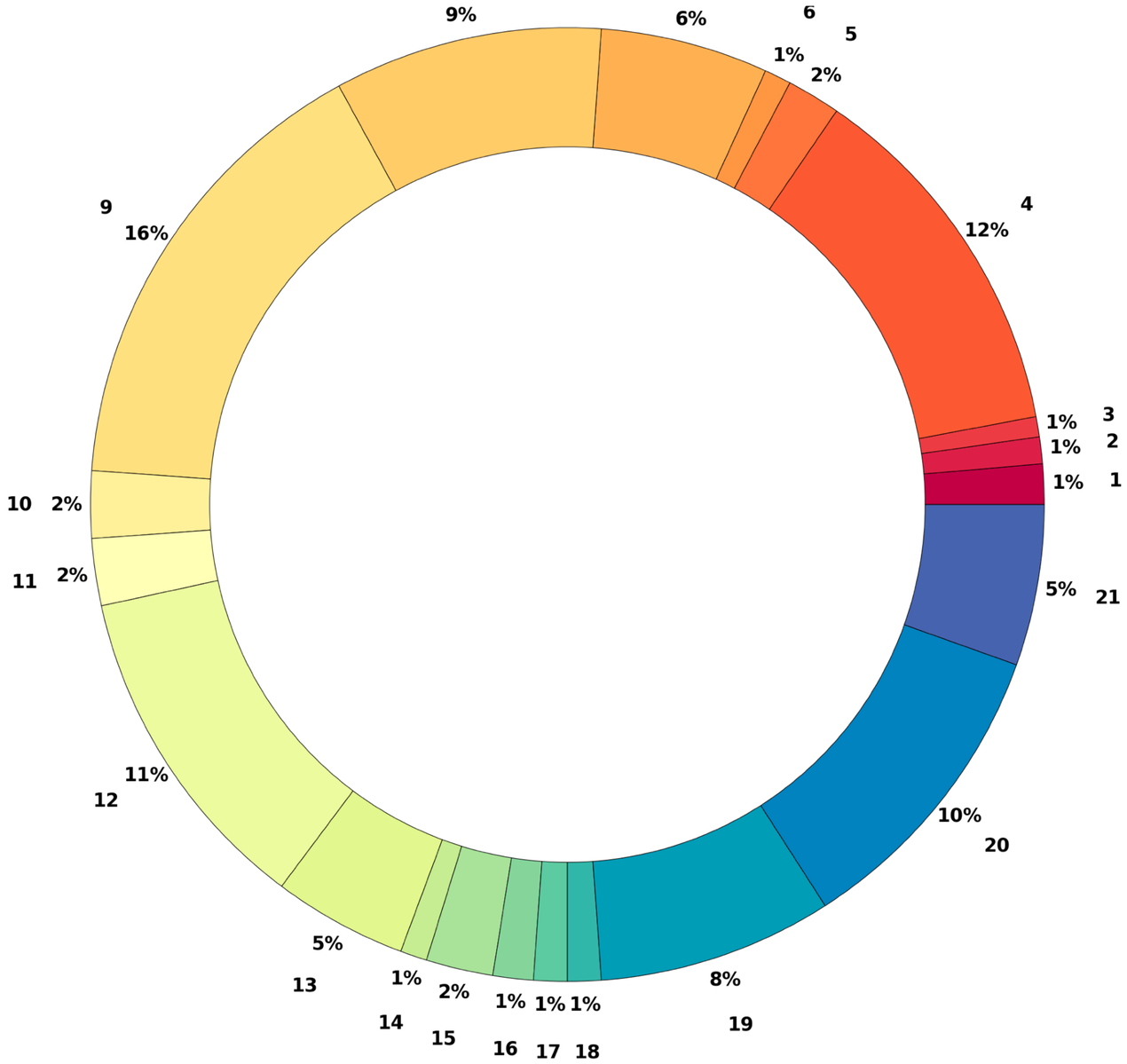




TDAC trimming



How long it takes ? time-breakout



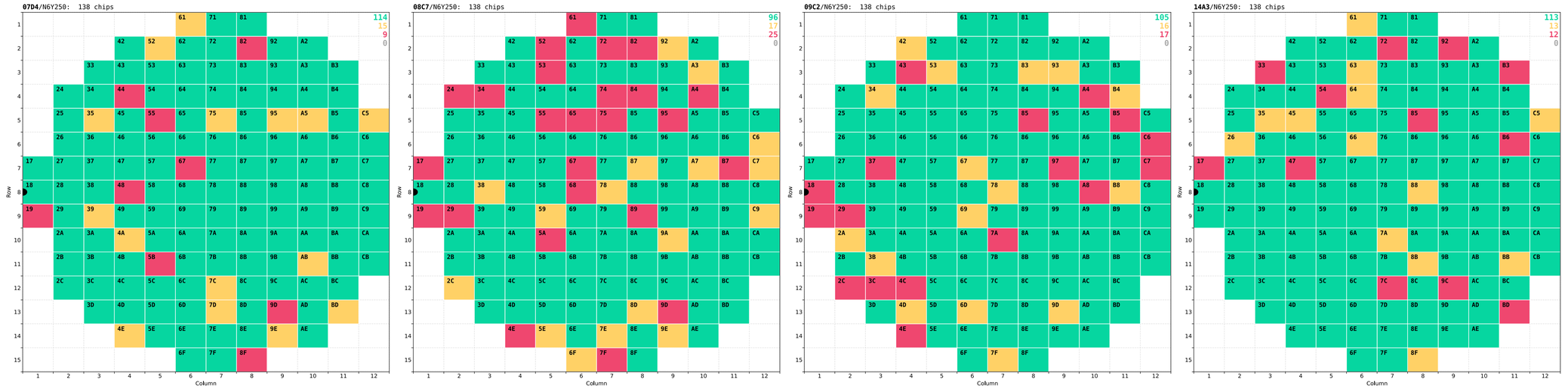
- IREF trimming (1)
- Startup communication (2)
- Writing efuses (3)
- VDD trimming (4) *
- Global registers (5)
- Injection capacitance (6)
- ADC calibration (7)
- DAC calibration (8)
- T sensors calibration (9) *
- Pixel power consumption (10)
- LDO IV curve (11)
- SLDO IV curve (12) *
- Aurora lanes (13)
- Chip ID (14)
- Pixel registers (15)
- Data merging (16)
- Digital scan (17)
- Analog scan (18)
- Coarse threshold scan (19)
- Threshold tuning (20) *
- Fine threshold scan (21)

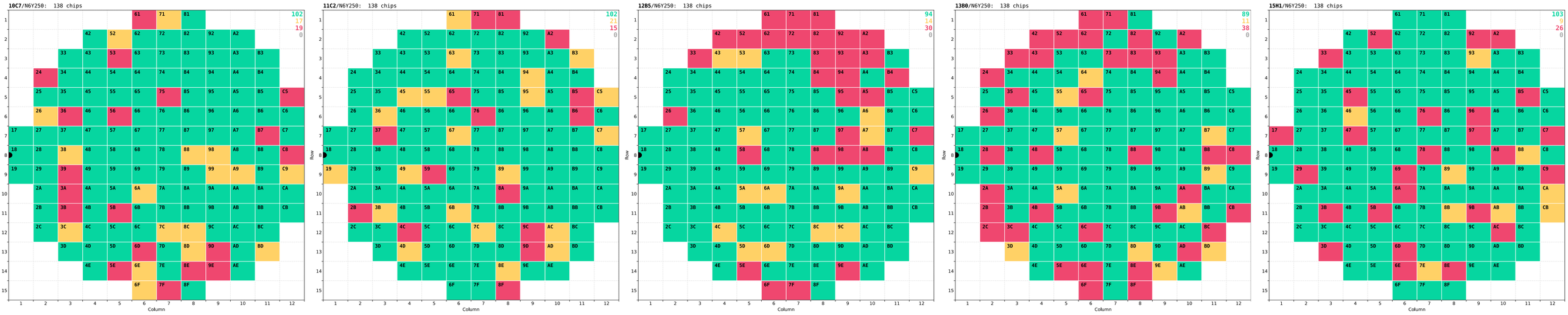
Testing one DUT takes in average 500s

For a whole wafer (138 chips) takes around 19h - that means you can test it in one day: compatible with 1.5y of testing, two centers, and with margins

Time optimisation still to be done. Also Scan-chain might replace few other test

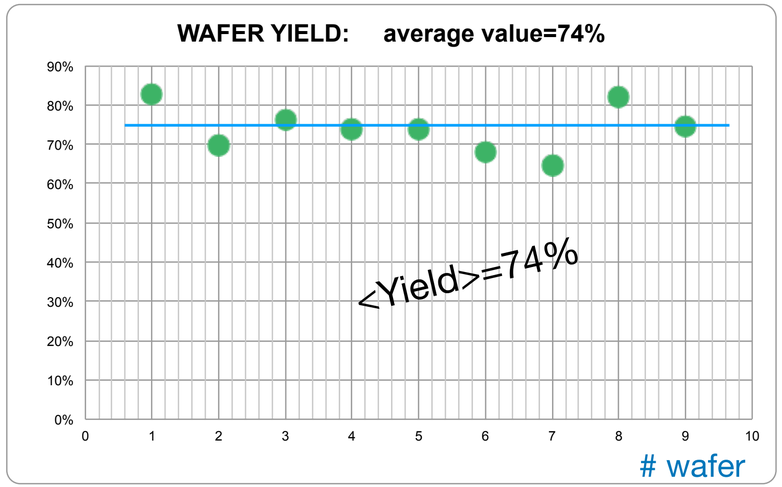
Wafer maps





only green CROC will go to CMS-IT modules

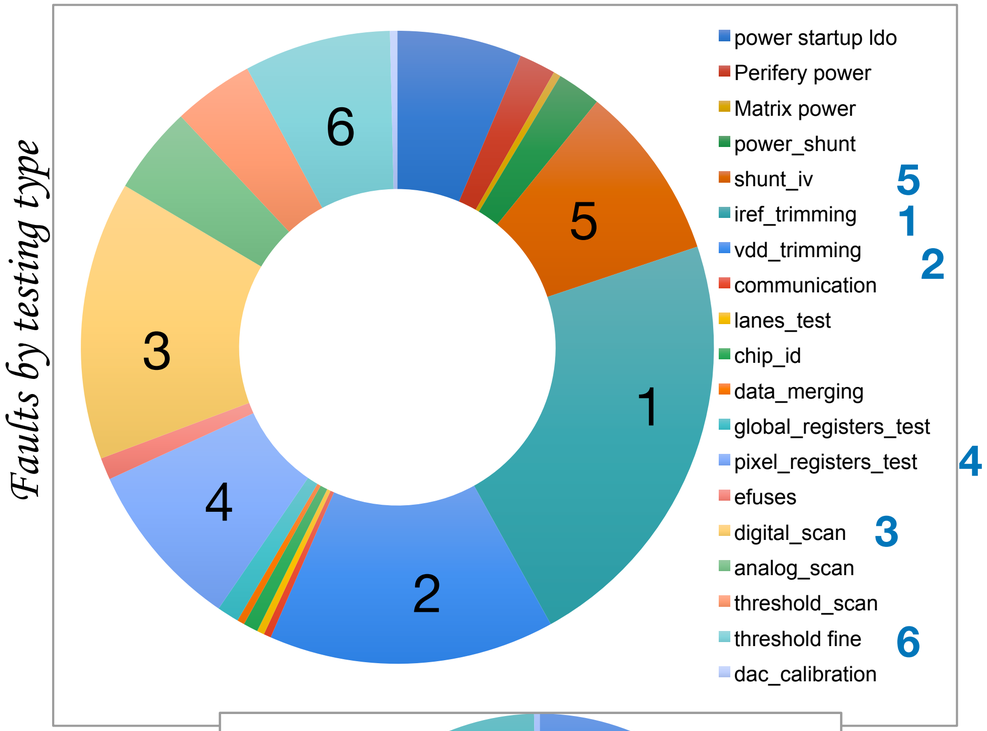
Yield and faults breakdown

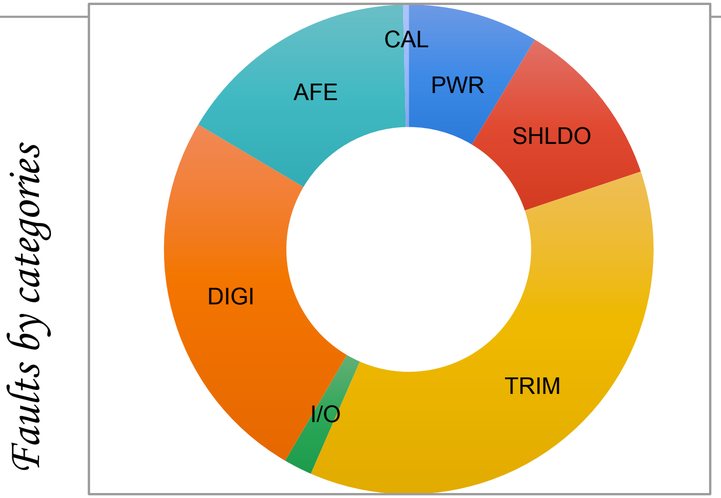


With the results obtained with wafer testing so far we measure a Yield of 74%. About 11% of those are Yellow chip that can be used for CROC characterisation / tests in laboratories.

A detailed breakdown of the contributions to the 26% rejection shows that major contributors are, in decreasing order :

- the TRIMMING (IREF, VDDx): to avoid low or high VDDA/VDDD before configuration (<1.1V, >1.3V) before or after irradiation (irradiation increases VDDx).
- It follows the digital scan and the pixel register, as precaution of avoiding defects on the complex digital-CORE and readout.
- third contributions is analog-front end (mainly noise, threshold tails)
- fourth contributions are PWR problems and SHLDO





Conclusions

- **Prototype CROC wafers arrived Fall-2021**. A wafer testing setup have been developed in Torino using the CMS-DAQ hardware: a new probe-card and ancillary boards have been built to allow full testing of the DUT and a specific wafer testing software have been designed. One CROC wafer have been dedicate to the setup commissioning / evolution / definition of testing procedures
- Three campaigns of testing have been done, according to the request of the experiment (chip dicing for characterisation / wafer for Bump-bonding vendors). **Eleven wafers have been measured**
- CROC selection criteria with specific cuts have been defined together with experts on CROC designers, testing , system tests, module production. The **yield** obtained is **of 74%** that can go for module assembly, 11% are yellow chip and 15% are defective chips.
- Testing **one wafer takes 19h**, compatible with the schedule of final-CROC production for the construction of the CMS Inner Tracker, tking into account equipping two centers
- Additional work still needed.
    - two tests to be finalised, the multilane Aurora and the scan-chain testing
    - testing time optimisation
    - feedback from prototype module production / system tests for cuts / measurements and calibrations needed
- Final **CROC submission planned for April-2023**

Backup

Scan chain test

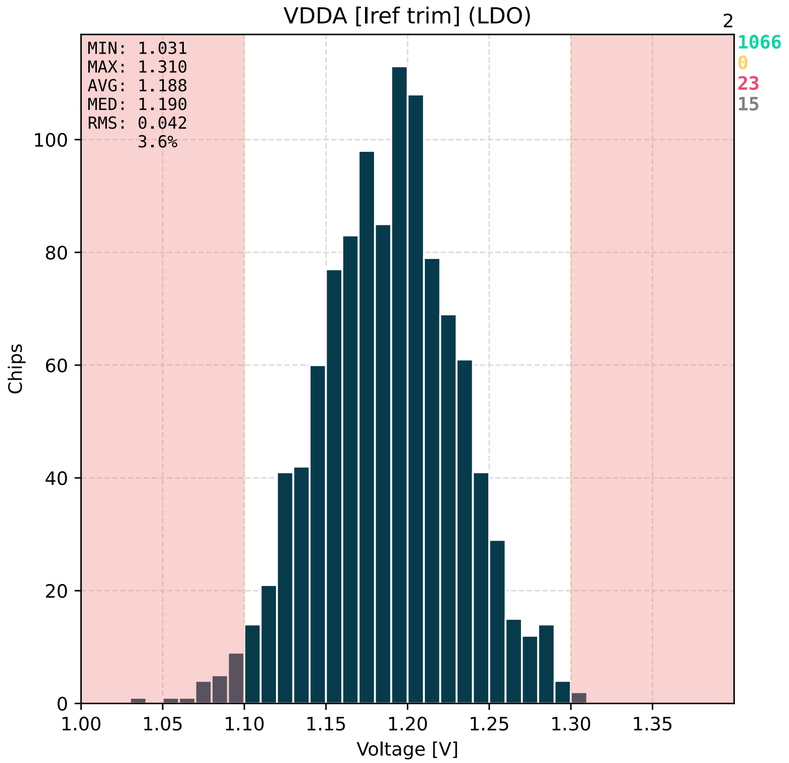
The RD53B has two main digital domains: Chip Bottom and Pixel Matrix. The Chip Bottom controls all functions of the circuit and any fault in it will affect the whole chip. Therefore, maximum test coverage is desired for the chip bottom. To achieve this, it has been synthesized with automatically inserted DFT features in the full logic code

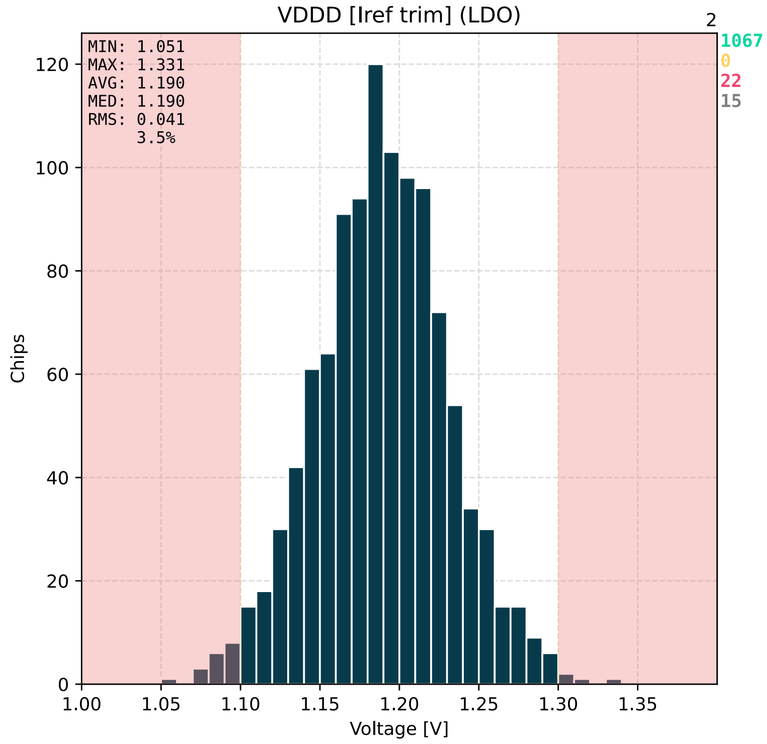
A scan chain is an industrial standard technique used in design for testing. The objective is to make testing easier by providing a simple way to set and observe every Flip-Flop in the Integrated Circuit.

CMS Tracker DAQ has developed a first version of scan-chain for Chip Bottom and Kansas State University is continuing the effort to make it efficient and fast for wafer level testing.

- 2033 vectors, each with 312111 bits are sent to the digital logic with a frequency of 8 or 20 MHz

IREF trim test





In the IREF test you want to avoid that at the startup the chip voltage goes above 1.3V or is below 1.1V