

Production and Testing of the Powerboard for ATLAS ITk Strip Barrel Modules

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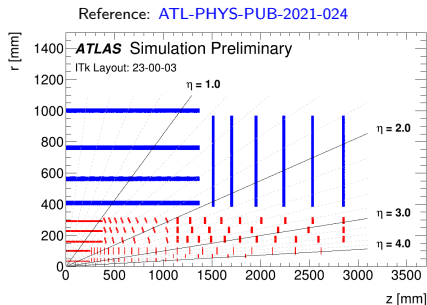
Lawrence Berkeley National Laboratory

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TWEPP 2022

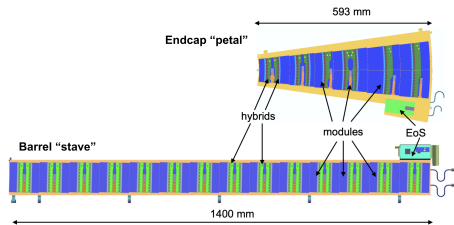


ATLAS ITk strip layout



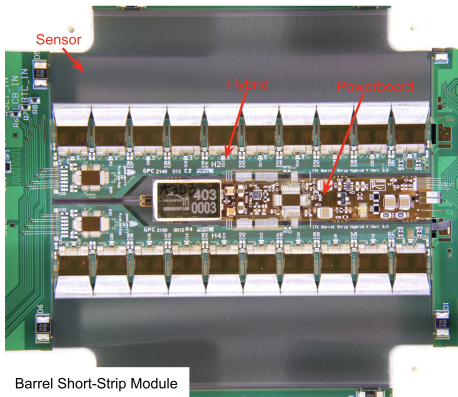
- Strip layers shown in blue
- 4 layers in barrel
- 6 disc layers for each endcap

Reference: [ATLAS-TDR-025](#)



- Two inner barrel layers have short strips (2.4 cm strips)
- Two outer barrel layers have long strips (4.8 cm strips)

ITk strip barrel module



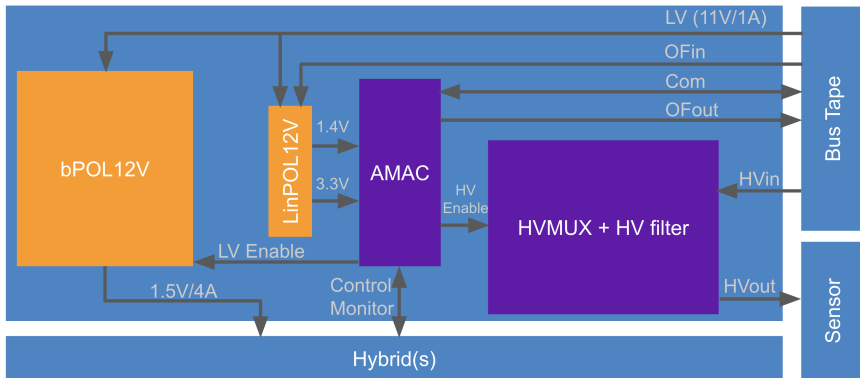
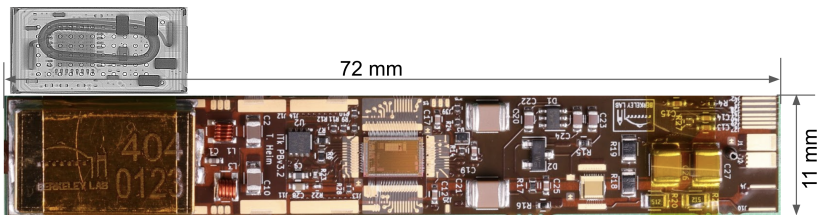
- Sensor
 - 98 mm x 98 mm
 - 4 (or 2) x 1280 strips with 75.5 μm pitch
- Hybrid(s)
 - 10 FE chips (ABCStar); each reads out 256 strips
 - 1 Hybrid Controller Chip (HCCStar)

- Powerboard
 - DC-DC converter (11V \rightarrow 1.5V) for hybrid(s) power
 - HV switch for sensor bias
 - Control and monitoring via custom ASIC (AMACStar)

Powering scheme

- Baseline powering scheme: **parallel power with DC-DC**
- Goal: deliver LV (1.5V @ 4A) and HV (500V @ ~mA) to 14 modules on a stave side with individual control
- Low-Voltage
 - One LV line per stave side at 11V
 - On module DC-DC conversion from 11V to 1.5V
 - Custom buck converter (bPOL12V) used due to strong magnetic environment, radiation requirement, low mass requirement
- High-Voltage
 - 4 HV lines per stave side, each shared by groups of modules
 - Individual module HV control/monitor by powerboard:
 - Switching via a HVMUX circuit by GaN FET (see presentation from [Luis Felipe Gutierrez Zagazeta](#))
 - Return current measured by AMAC

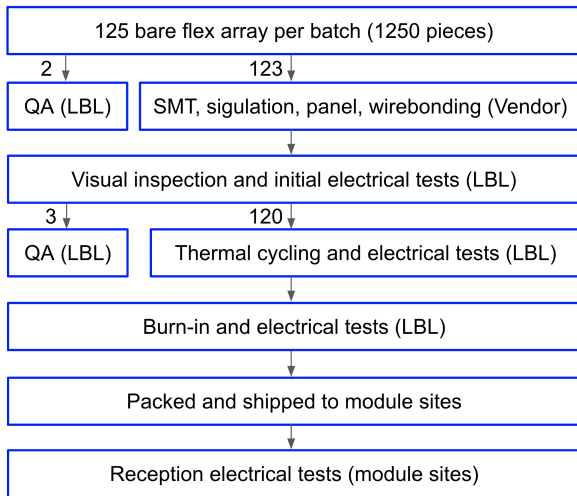
Powerboard design



Production status and plan

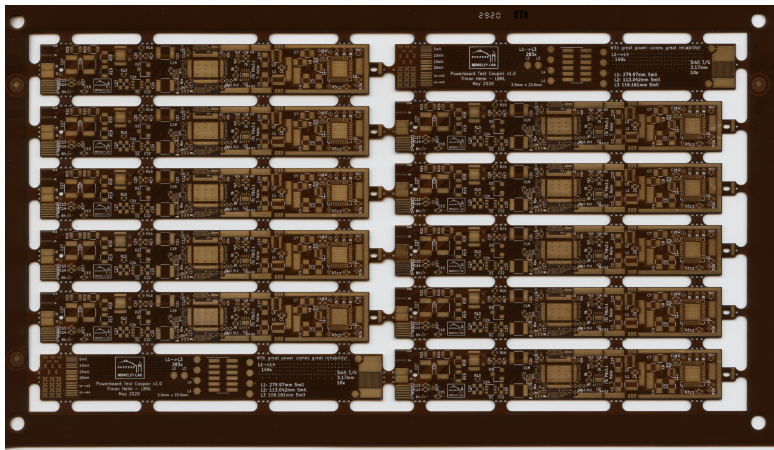
- Pre-production is finished
 - PPA: 250 powerboards; PPB: 850 powerboards
 - Main powerboard part change from PPA to PPB: AMACv2a to AMACStar, with improved SEE mitigations (see presentations from [R. Roberts](#) and [A. Wall](#))
 - Half of PPB powerboards are produced at full production speed and tested with full QC procedure
- Production will start after Production Readiness Review (PRR, late 2022)
 - In total need to produce and test about 14,100 powerboards in two years

Production and testing flow



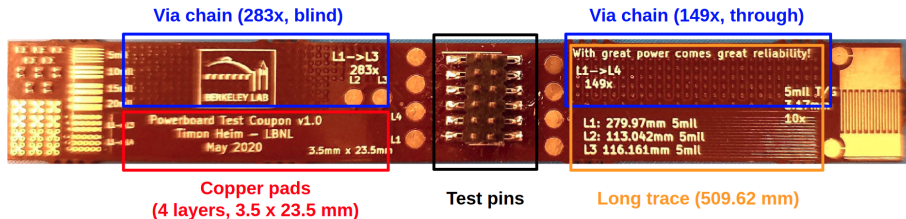
- Initially we planned to do QC tests by vendor as well, but eventually decided to move them to LBL due to lack of expert support at vendor

Powerboard flex array

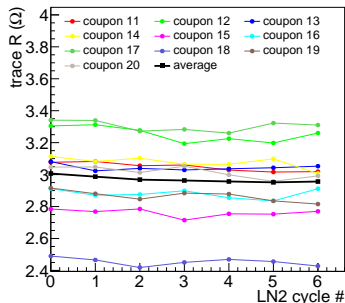


- 4-layer flex PCB, total thickness: 16.7 mil
- Smallest track width: 5 mil; minimum via: 6/16 mil; smallest SMT package: 0201

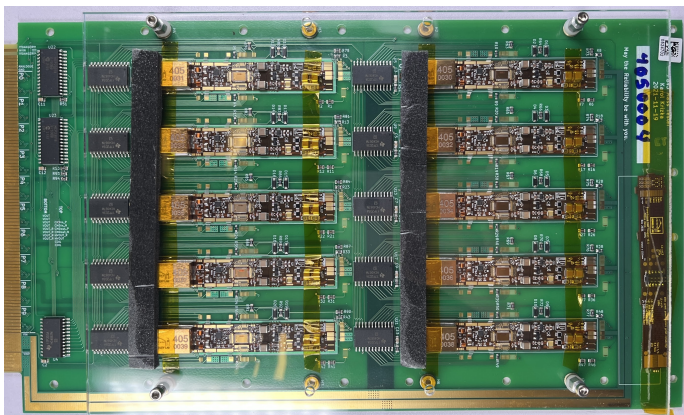
QC and QA for flex material: test coupon



- Test coupon: a proxy of the powerboard flex material
- 2 test coupons are produced for every 10 PBs, with 1 coupon reserved for QC/QA
- QC tests: resistance of via chains/long trace; capacitance between copper pads, breakdown voltage of trace gap
- QA tests: thermal shock, irradiation



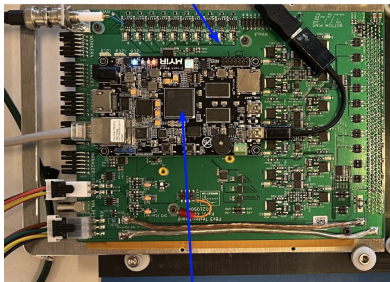
Powerboard carrier card



- After SMT loading, powerboards are singulated from flex array and loaded to carrier cards for wirebonding and electrical tests
- Need to produce more than 1000 carrier cards: to reduce cost, only necessary MUX are on placed on carrier card, testing circuits placed on a reusable PCB (active board, next slide)

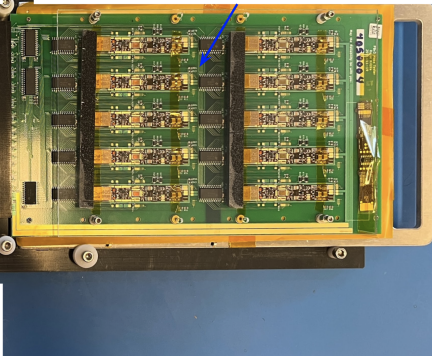
Electrical test system

Active board: circuits for all electrical tests, reusable



ZTurn SoC board: holds and runs all testing programs

Powerboard carrier card: holds 10 PBs
Connected to PBs via temporary bonds



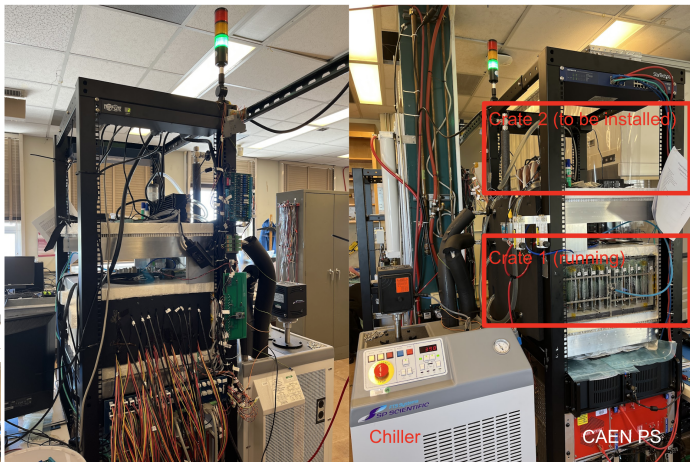
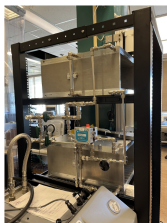
- Electrical tests: basic functionalities and characterizations of LV/HV/AMAC
- The system is used for 10 module production sites for reception tests
- The system is also used for massive tests during production QC

QC procedure and requirements

- After assembly, each powerboard will go through QC, which includes: visual inspection, thermal cycle, burn-in, and electrical tests (both at warm and cold conditions) in between steps
- Thermal cycle: cycle the powerboard temperature between -35°C and 40°C for a few times
- Burn-in: load each powerboard at 2 A for 24 hours without interruption
- Requirement for the QC system:
 - Cooling requirement: powerboard temperature down to -35°C
 - Safety requirement: prevent over-heating, condensation, etc.
 - Speed requirement: 150 powerboards per week

Crate for powerboard QC

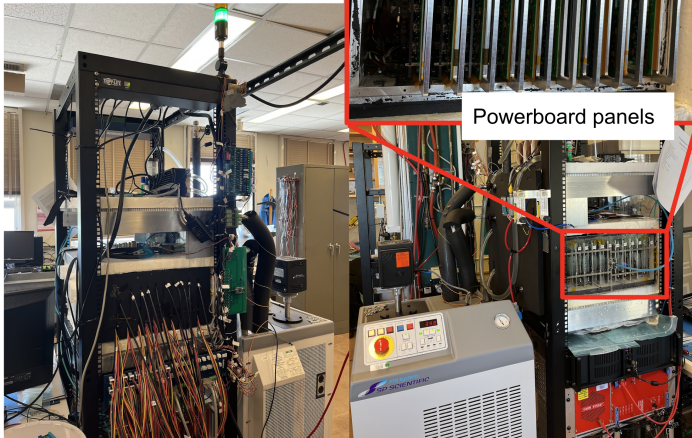
- Two crates in one rack, sharing the same chiller and power supply system
- Each crate can test 100 powerboards at a time



A second rack (with two crates) is being installed for QA/backup for QC.

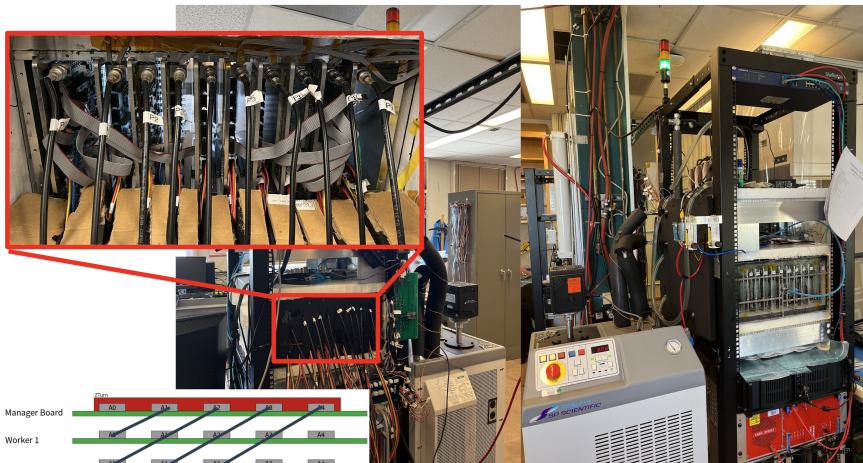
Crate for powerboard QC

- 10 panels (100 powerboards) per crate
- Each panel connects to an active board for electrical testing (at the back side)



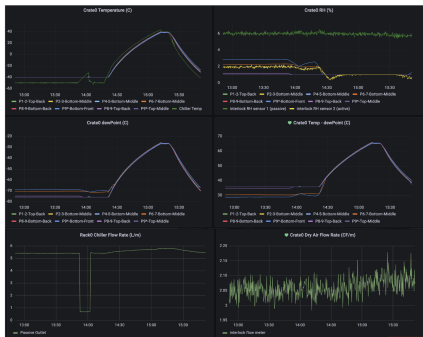
Crate for powerboard QC

- Water cooling + fan used for active board cooling

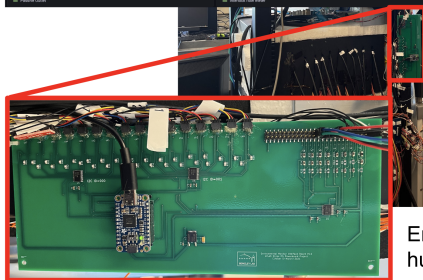


- 10 active boards, managed by 2 ZTurn SoC
- Each ZTurn controls 5 active boards

Crate for powerboard QC



Environmental board monitors the temperature, humidity, air and fluid flow speed in the crate

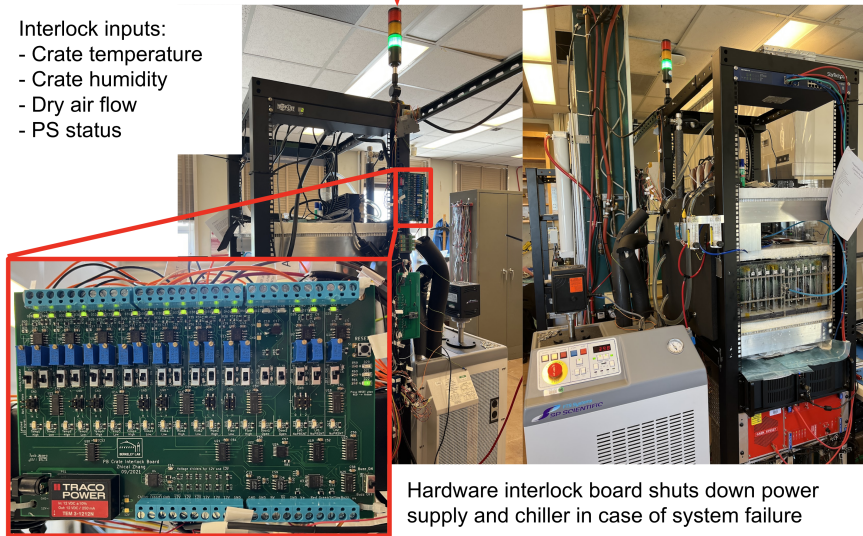


Crate for powerboard QC

Light tower with loud sound alarm

Interlock inputs:

- Crate temperature
- Crate humidity
- Dry air flow
- PS status



Hardware interlock board shuts down power supply and chiller in case of system failure

QC software

- All QC steps are fully automated and integrated into an all-in-one custom web-based GUI, with minimum human attention required (a few button clicks per day): the GUI includes database interaction, electrical testing program and result display, chiller operation and temperature monitoring

Panel number: APPE FILL

Powerboard Version Number: Powerboard Batch Number

Board 0: Board 1
 P50 Serial Number: P51 Serial Number

Board 2: Board 3
 P50 Serial Number: P50 Serial Number

Board 4: Board 5
 P50 Serial Number: P50 Serial Number

Board 6: Board 7
 P50 Serial Number: P57 Serial Number

Board 8: Board 9
 P50 Serial Number: P50 Serial Number

Upload Test Results

Panel Start Transition To: Module Reception

None
 Debug
 Super Debug

SYSTEM INSTALLATION

RUN BASIC FUNCTIONALITY TEST RUN CHARACTERIZATION TEST STOP TEST

STATUS load (A) time (S)

Jump to:

- Basic Functionality
- Generic Tests
- ASIC Tests
- DC/DC Tests
- HV Tests
- Thermal

Basic Functionality Tests

Powerboard	Pal ID	SER	LIMPLY (V)		DC/DC Out (V)		HV In Current (A)		HV Out Current (A)		What (counts)	
			OFF	ON	OFF	ON	OFF	ON	OFF	ON	OFF	ON
0	0	1.00	0.17	1.42	0.00	1.47	4.8e-7	8.8019	1.5e-7	8.8004	136.00	459.00
1	0	1.00	0.17	1.42	0.00	1.45	9.8	8.8019	1.2e-7	8.8004	148.00	475.00
2	0	1.00	0.17	1.42	0.00	1.46	9.8	8.8019	1.5e-7	8.8004	157.00	569.00
3	0	1.00	0.17	1.42	0.00	1.46	9.8	8.8019	1.7e-7	8.8004	156.00	468.00
4	0	1.00	0.17	1.41	0.00	1.53	9.8	8.8019	8.2e-8	8.8004	157.00	465.00
5	0	1.00	0.17	1.40	0.00	1.48	9.8	8.8019	1.7e-7	8.8004	145.00	482.00
6	0	1.00	0.16	1.42	0.00	1.58	9.8	8.8019	1.7e-7	8.8004	146.00	471.00
7	0	1.00	0.16	1.42	0.00	1.58	9.8	8.8019	1.5e-7	8.8003	144.00	476.00
8	0	1.00	0.16	1.44	0.00	1.48	9.8	8.8019	1.4e-7	8.8003	155.00	507.00
9	0	1.00	0.16	1.35	0.00	1.51	9.8	8.8019	1.4e-7	8.8004	151.00	459.00

Basic Chiller Operations

Order is On

TURN ON CHILLER TURN OFF CHILLER

SET TARGET TEMPERATURE (C): set-temp SET TARGET TEMPERATURE (F): 80

SET RAMP RATE (C/MINUTE): set-temp SET RAMP RATE (C/MINUTE): 0.5

MEASURED CURRENT TEMPERATURE (C): 10.00 START MONITORING STOP MONITORING

Save to CSV Save to InfluxDB

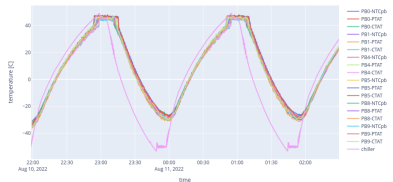
Thermal Cycle Settings

Low Temperature (C): -60 High Temperature (C): 40 Ramp Down Rate (C/minute): 0.5 Number of Cycles: 5

LowTemp keep time (minute): 10 HighTemp keep time (minute): 10 Ramp Up/Fall (C/minute): 0.5 End Cycle Temp (C): 00.0

START NORMAL CYCLE STOP NORMAL CYCLE

cycle info: 3, used time 00:01:14, remaining time: 2:37:24



Observations of QC during pre-production

- We have exercised the full QC procedure with one crate on PPB powerboards:
 - One crate can test 100 powerboards per week (400 tested in total)
 - Eventually we'll have 2 crates for QC and 2 crates for QA/backup
- Half of the time spent on thermal cycle and burn-in, the other half spent on electrical tests:
 - In total 5 runs of electrical tests are implemented before and after thermal cycle/burn-in (including test runs at warm and cold)
 - One run of test for one panel takes about 1.5 hours
 - Fully parallelization of testing of 10 panels in a crate turned out to be difficult due to communication traffic restrictions with the CAEN PS system (lots of LV/HV scans)
 - In practice we spent about 4 hours for each test run
- A technician is needed to babysit the QC: click buttons a few times a day, examine test results, book-keeping, etc.
- Testing system runs smoothly during the one month exercise: no system failure/interlock, no expert interruption needed

Summary

- Powerboard is a critical component for the ITk Strip module: power, monitor, control
- Production of $\mathcal{O}(10000)$ such boards with high reliability is a big challenge
- Fully industrialization turned out to be difficult due to lack of expert at vendor
- We presented a production QC system to be run in our local lab:
 - QC testing programs: thermal cycle, burn-in, electrical tests
 - Fast testing speed: fulfill the 150 boards/week schedule
 - Automation: all-in-one testing GUI, only requires a few button clicks/day
 - Desired safety: fully hardware interlock system
 - Cost effective: maximum reusable testing parts, minimum human interruption
- The QC system has been proved working smoothly during pre-production of powerboards
- Production of powerboards will start soon

Backup slides

Testing circuits on active board

Powerboard

Active Board

Carrier Case

Active Board

Variable loads

HV current measurement

Monitoring ADC (VOUT, V_NTC)

Pick up coil MUX

AMAC command MUX

max VDAC = 3.3 V
voltage divider = 0.14
max VSETI = 0.48 V (4.8A load)
8 bit DAC = 19 mA / count

U401B

TLV274

Q403 NTD4858N

5 W at max load

2.5 W at max load

VOUTO

VSETO

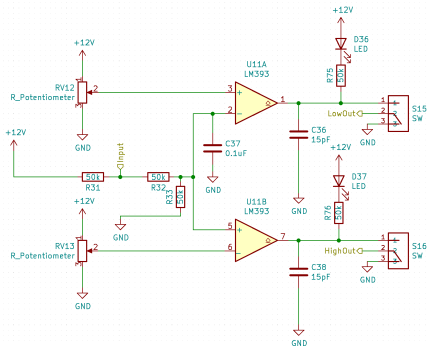
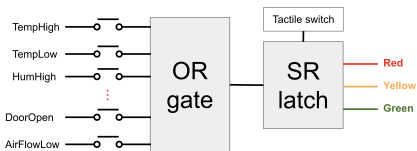
VOUT_RTNO

GND

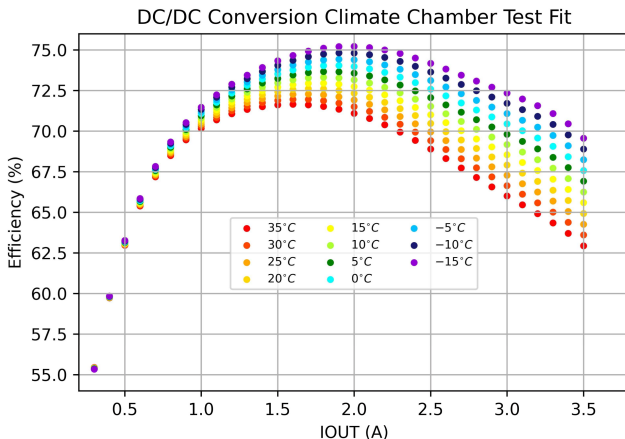
- For details of each testing circuit, see [our poster on TWEPP 2021](#)

Hardware interlock

- Pure hardware interlock with capability to monitor generic analog input signal



Recent results: DCDC efficiency (Preliminary)



- Efficiency of the latest version (bPOL12V_v6) is measured on powerboard in a climate chamber
- Operated at 2.2 MHz switching frequency with a ~ 250 nH coil
- Target efficiency (60-70%) obtained for desired loads

Recent results: DCDC noise (Preliminary)

- bPOL12V running at switching frequency around 2MHz
- Shield box + shielding layer on powerboard acting as Faraday cage mitigating EMI noise reaching the sensor
- Two measurements performed on the bPOL12V noise (via oscilloscope):
 - Direct measurement of noise amplitude of VOUT
 - Measurement by pick up coil on carrier card

