New readout electronics for ATLAS ZDC detector

In this paper we presented LHC Run3 upgrade of the readout electronics chain for ATLAS ZDC detector. The ZDC detectors are located in the LHC tunnel on both sides of ATLAS IP and designed for detecting far-forward neutrons from interactions during lead-lead collisions. From each side ZDC send 4 signals by the 200m air-core cable to the ATLAS counting room. Replacing former CC50 cables allowed to sharpen the shape of the signals arriving at new electronic modules and locate them within the 25 ns (single BCX) time window permitting separation of original signals from the pileup.

The new ZDC-LUCROD readout module, originally designed for the LUCID detector, is a 9U VME board capable of processing signals from 8 channels with a FADC sampling rate of 320 MHz. To allow for a larger amplitude's dynamic range the signals from both sides enter one board (LowGainThresholds) and after programmable amplification are fed into inputs of another board (HighGainThresholds). The first 4 channels of the board are assigned to side A and the remaining 4 to side C.

The ZDC-LUCROD modules were also modified to produce ZDC digital triggers. To efficiently identify a peak in the signal as a candidate for a trigger the module has been equipped with online calculation of the second derivative. The 12 bit FADC detector samples undergo subtraction of a baseline values assumed to be the first sample from the programmable time window. Profiting from the pipelined operation the 2^{nd} derivative is then calculated. The 2^{nd} derivative going above a threshold indicates a pulse. Presence of a pulse starts a search in the time window for a maximal ADC value. The further processing calculates arithmetic average of the 4 channels from each side. This average is then used in first level of LUTs to produce a 4-bit output. In the final step the 4-bit outputs from both sides are used in another level of LUT to produce 3-bit final trigger code sent to CTP. The thresholds used to classify pulses when accessing the first level LUTs and the contents of all LUT are programmable. The trigger performance was tested during the LHC Pilot Beams in 2021 and it shows perfect matching with the off-line analysis of data.

The full integration with the ATLAS TDAQ required s-link interface and firmware to handle Level-1 Accept requests. The ZDC-LUCRODs send data to ATLAS Readout System (ROS) via the s-link fiber with ATLAS formatting (ROD headers). The VME access to various registers and memories is used to monitor operation of the module. The modules can also generate a BUSY to avoid data loss in case the s-link throughput is saturated by bursts of triggers. The module is also equipped with Level-1 Accept pipeline where samples await a decision. In case of the positive decision data from a number of BCXs can be accessed and forwarded to the s-link channel. In case of module's desynchronization the TTCrestart procedure can be executed to reintegrate the module into a running ATLAS TDAQ.