

Pre-Production Testing of the AMACStar ASIC at Penn for the ATLAS ITk Detector

Thomas Gosart on Behalf of the ATLAS ITk Collaboration

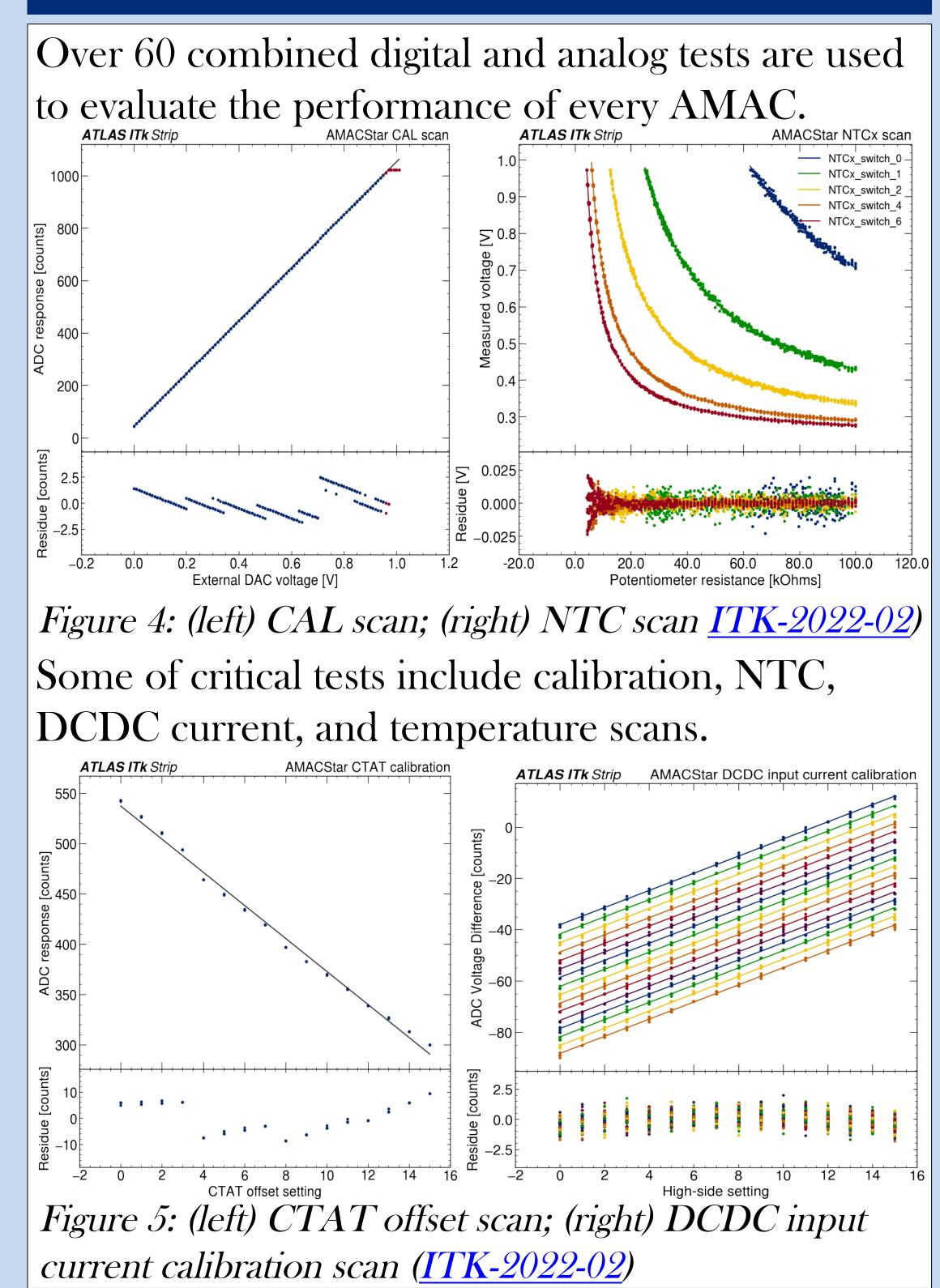
Testing the AMACs



Abstract

The high-luminosity upgrade to the LHC (HL-LHC) requires a new inner detector, the Inner Tracker (ITk) detector. AMACStar is one of three application specific integrated circuits (ASICs) that will be installed on the ITk strip modules.

--- 18000 AMACStars will be produced



Pre-Production and Priming Results

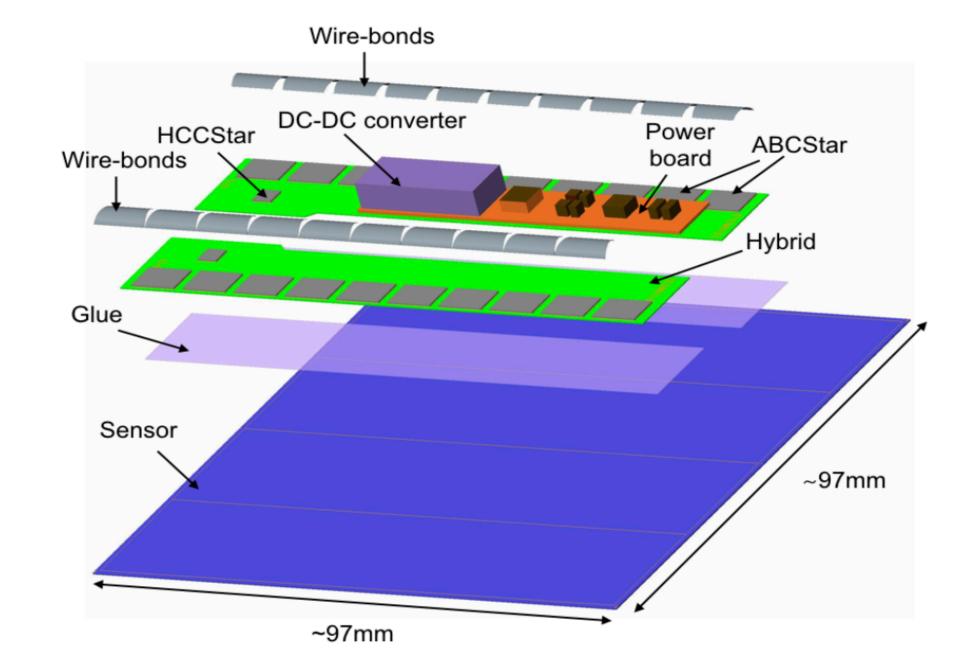
Grading parameters are used to assess the digital and analog performance of a given AMAC after we run our tests.

Grade	Description	
Good (A)	Passed all digital and analog	
	parameters	
Accept (B)	Passed all digital and vital	
	analog parameters	
Bad (F)	Failed 1+ digital or vital analog	
	parameters	

- --- Wafers of these chips are tested at the Penn probe station
- --- A comprehensive testing suite and grading scheme is applied to each chip The results from the pre-production satisfy the required 90% yield needed for production goals.

ATLAS ITk

The ITk detector will replace the existing ATLAS tracker system. The ITk strips subsystem will be made of silicon modules. The modules are made up of silicon sensors and readout electronics, including three ASICs: the ABC (ATLAS Binary Chip), HCC (Hybrid Controller Chip), and AMAC chip (Autonomous Monitor And Control) [1].



3 wafers were probed for pre-production and 8 were used for production priming. Based on the detector requirements, a yield of 90% 'Good' chips is expected per wafer. We reached this goal during both, the pre-production and priming phases.

	Good	Accept	Bad	
Wafer #1*	486 (99.8%)	0	1 (0.2%)	
Wafer #2	447 (91.8%)	26 (5.3%)	14 (2.9%)	
Wafer #3	473 (97.1%)	6 (1.2%)	8 (1.6%)	
Priming	92.63%	4.65%	2.72%	
*Only a fraction of the final parameters were				
developed for this wafer				

A total of 68 digital and 262 analog parameters were reviewed and deployed for the production priming wafers. This process finalized the testing suite and grading scheme for production.

Figure 1: Schematic of an ITk strips module

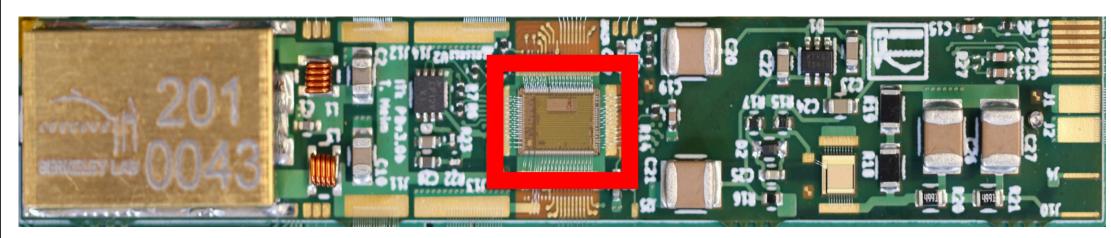


Figure 2: Image of a power board [2]. The AMAC chip is located directly in the center

The AMACStar Chip

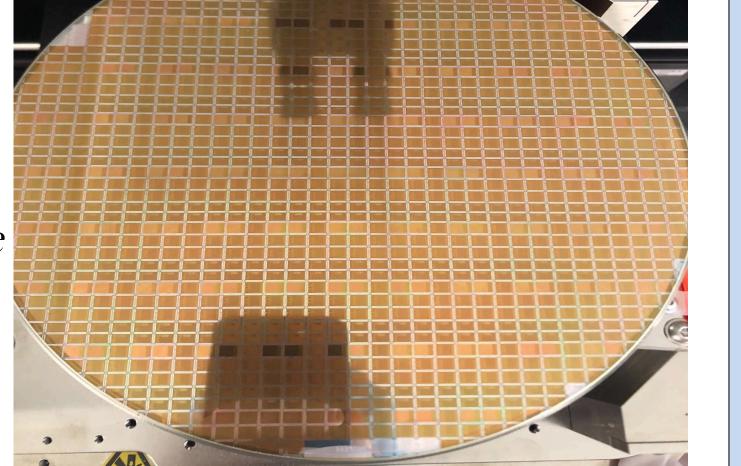
The AMACStar chip contains a 16 channel ADC and interlock mechanism. It autonomously monitors temperatures, voltages, and currents and controls the module [3]. If vital quantities become too high, the chip can flag these issues and disable voltages. Figure 3: Image of a single AMACStar chip

Penn Probe Station

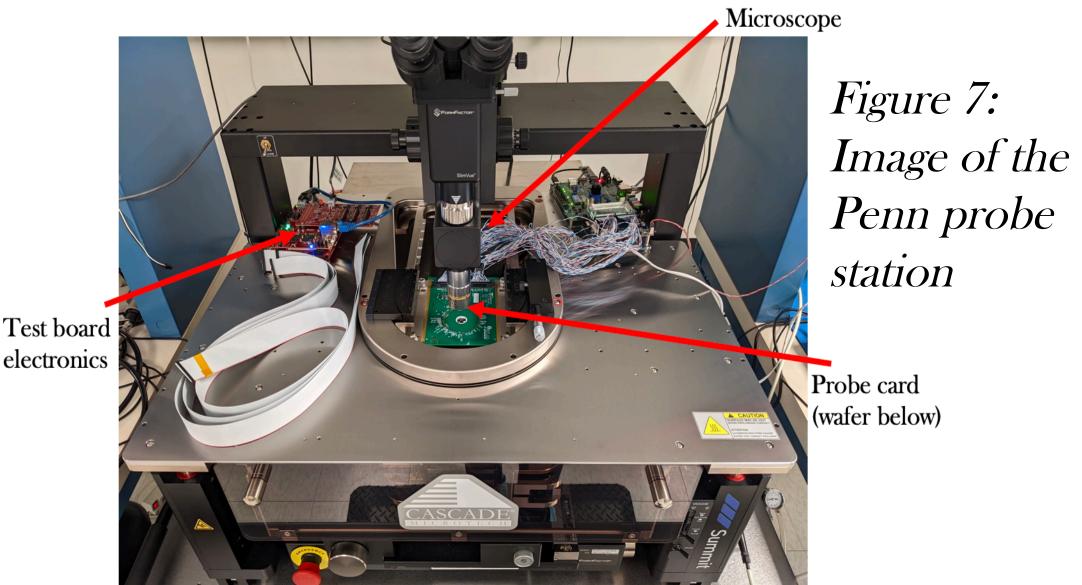
We use a probe station inside a clean room at Penn to probe shared wafers of HCCStar and AMACStar

chips.

Figure 6: A shared wafer of HCCStar and AMACStar chips loaded in the probe station



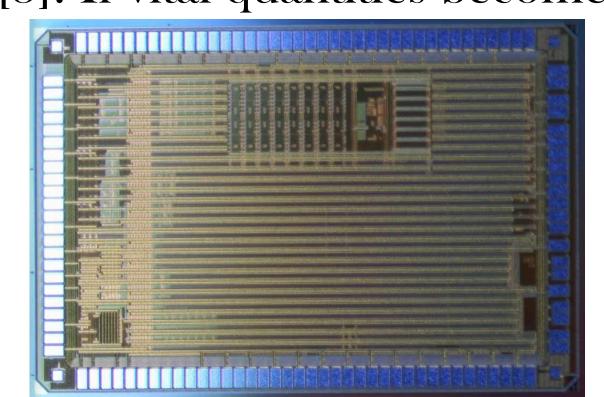
Each wafer contains 487 AMACStars, which take about 27 hours to fully probe. After probing every AMAC, each chip is assigned a grade: Good, Accept, or Bad.



ATLAS ITk Strip

438 439 440 441 442 443 444 445 446 447 448 449 450 451 452 453 454 455 456 4 431 | 430 | 429 | 428 | 427 | 426 | 425 | 424 | 423 | 422 | 421 | 420 | 419 | 418 | 417 | 416 | 415 | 414 | 413





gory B: 24 (4.9%) Logic Failure: 5 (1.0%) Analog Failure: 9 (1.8%) Comm Failure: 1 (0.2%) eFuseID Failure: 1 (0.2%)

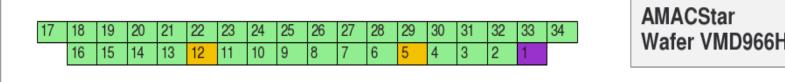


Figure 8: Example wafer map from one of the production priming wafers <u>ITK-2022-02</u>)

Conclusions and Future

Based on the strong performance of the AMACStar chip (as well as the HCCStar) throughout pre-production, the order for production wafers has been placed. The first batch will arrive in December 2022 and production is scheduled to begin in early 2023.

References

[1] ATLAS Collaboration, TDR for the ATLAS Inner Tracker Strip Detector, ATLAS-TDR-025. [2] Karol Krizka, "Results of the Powerboard for ATLAS ITk Strip Barrel Modules." TWEPP 2019. [3] ITk Strip Collaboration (2022) ATLAS ITk Electronics Specification: AMACStar ASIC: https://gitlab.cern.ch/atlasitkstrasic-group/AMAC/-/blob/star_doc/doc/Specification/AMACStar_Spec.pdf

tgosart3@sas.upenn.edu