Pre-Production Testing of the HCCStar at Penn for the ATLAS ITk Detector

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Abstract

The high-luminosity LHC requires a complete overhaul of the ATLAS inner tracker subsystem, including a new silicon-strip charged-particle tracking detector. The **HCC (Hybrid Controller Chip)** is one of three new radiation-tolerant ASICs for this subsystem. As the interface to multiple binary readout ASICs for the strip detector, the HCC buffers and forwards controls signals and trigger and readout requests to them, and serializes their output at 640 MHz. All HCCs undergo a suite of tests to verify their analog and digital functionality, and large statistics of performance with various operating parameters has been studied.

ITk Strip Detector and HCC

- ATLAS **Inner Tracker (ITk)**: silicon **Strip** and Pixel charged-particle tracking detector subsystems
- **HCC (Hybrid Controller Chip)**: an ITk Strip ASIC
  - Interface to up to 11 ABCs (ATLAS Binary Chip)
    - ABC provides 256 channel analog detector readout
  - Forwards clock/control signals to ABCs, including physics data readout requests, register read/write commands, calibration commands, and resets
  - Reads ABCs at 160 Mbps and serializes physics data output at 640 Mbps
- **HCCStarV1**: final version, star network readout, triplicated logic for radiation tolerance

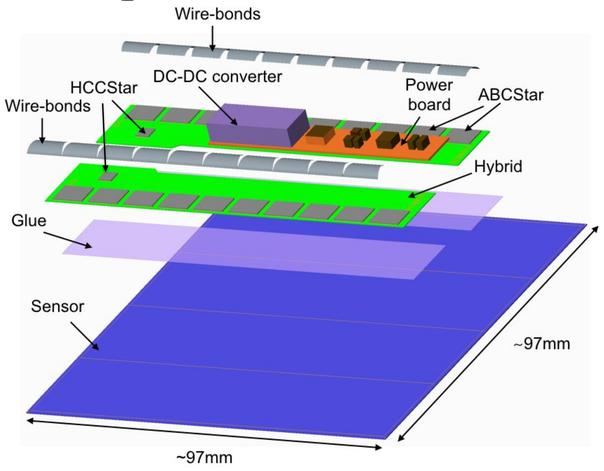

Fig. 1: An exploded view of an ITk Strip detector module. Note the two HCCStar chips on the top-left. (Source: ATLAS-TDR-025 on CERN CDS)

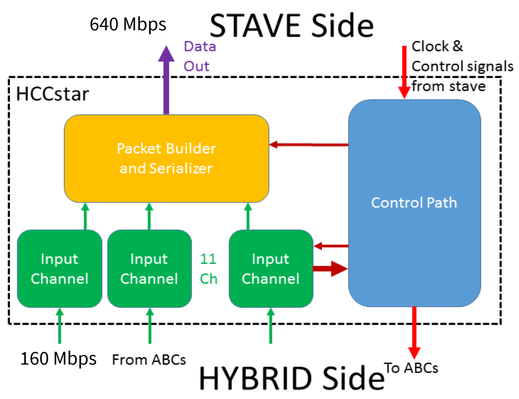

Fig. 2: A top-level block diagram of the HCCStar.

HCC Wafer Probing

- ASICs produced on mixed silicon wafers containing 557 HCCStarV1s
  - 25,500 HCCs for ITk Strip detector ⇒ ≥62 wafers needed
- Wafer probing procedure:
  - wafer mounted on Summit probe station in cleanroom
  - custom probe card contacts all input/output pads of individual HCC die on wafer
  - custom firmware communicates with chip to test digital & analog functionality
- Based on results, die marked as Category A, B or X (failing) for dicing and distribution
  - B chips usable but not ideal (*e.g.* high power draw)

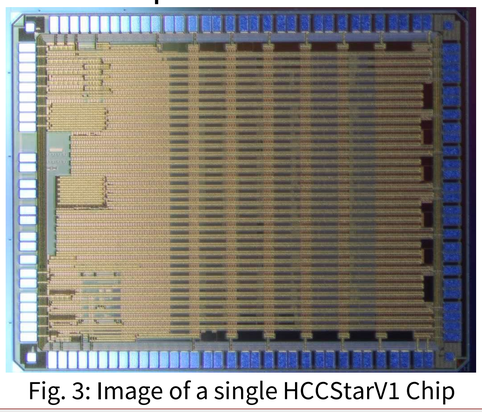

Fig. 3: Image of a single HCCStarV1 Chip

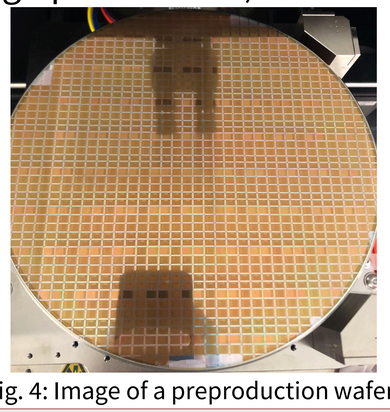

Fig. 4: Image of a preproduction wafer

HCC Probe Tests

The probe tests include the verification of important HCC functionality:

- **Analog**: ensure voltage regulator can achieve 80 mV above and below working point of 1.2 V, calibrate onboard ADC and use for remote monitoring of currents and voltages, compare with external ADC measurement
- **Trigger**: check that HCC receives and distributes trigger requests correctly, and receives and identifies errors in simulated ABC readback
- **Memory**: set and read registers and memory on HCC and simulated ABCs, check defaults after reset, ensure malformed commands ignored
- **Passthrough**: check that HCC correctly interprets and reformats messages for individual ABCs
- **Triplicated clocks**: disable individual triplicated clock signals and rerun critical subset of trigger and memory tests, to ensure that the individual paths of the triplicated logic functions properly

Probe Testing Results

- Engineering run of 12 wafers probed at Penn
  - 1 test, 3 preproduction, 8 production priming
- **Total yield of Category A HCCs is 96%**
  - Exceeds 90% yield of A plus B targeted for production
  - For priming: 96.0% A / 0.6% B / 3.4% X

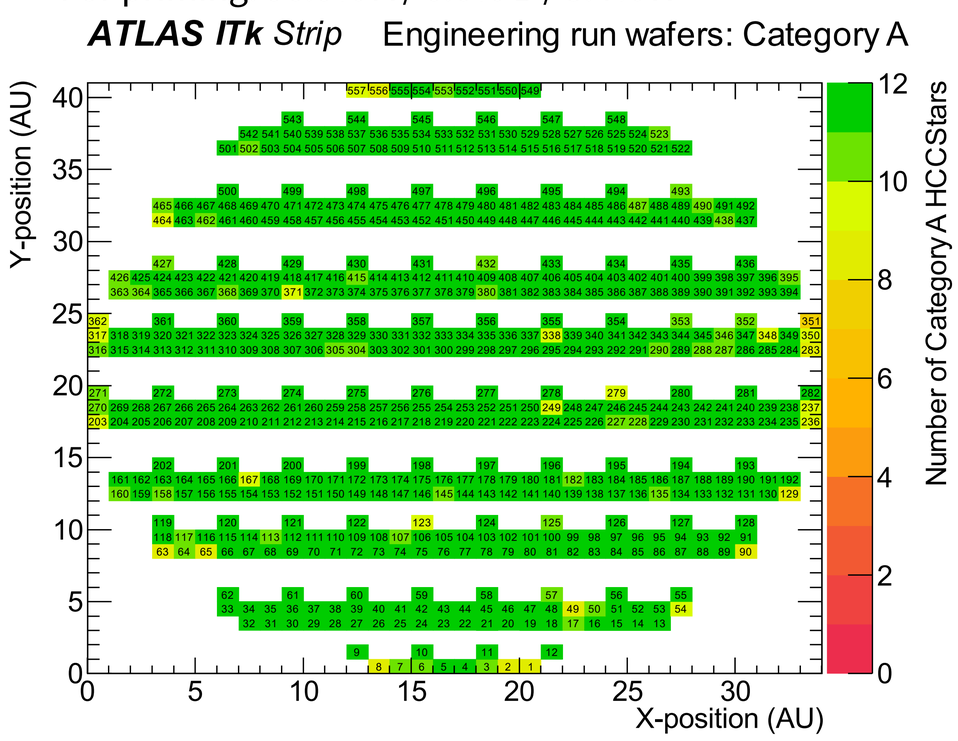

Fig. 5: Histogram of Category A HCC die locations on 12 engineering run wafers (Source: ITK-2022-002 on CERN CDS)

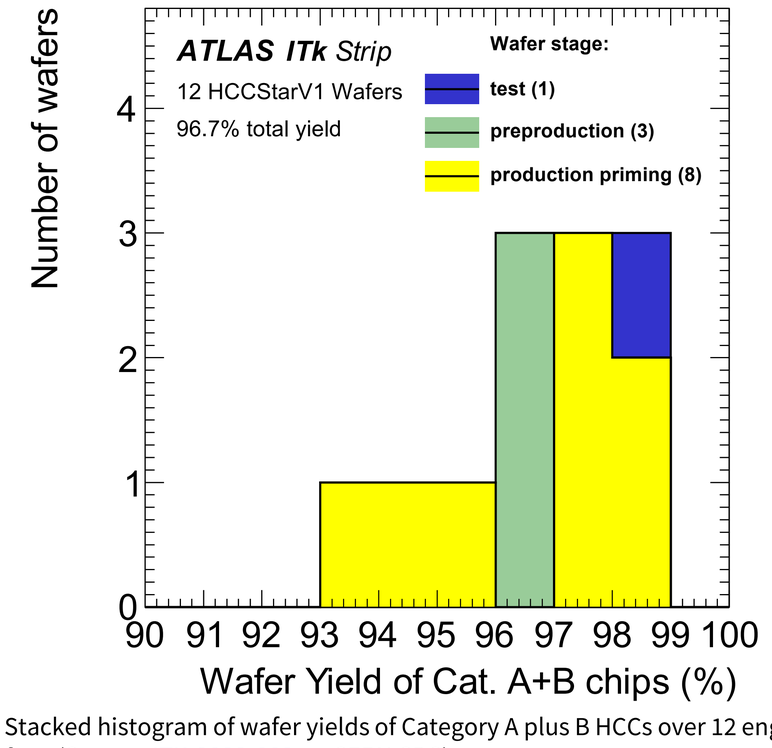

Fig. 6: Stacked histogram of wafer yields of Category A plus B HCCs over 12 engineering run wafers. (Source: ITK-2022-002 on CERN CDS)

For more information, see J.R. Dandoy *et al* 2023 *JINST* **18** C02026 (also available as ATL-ITK-PROC-2022-028 on CERN CDS).