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Pre-Production Testing of the HCCStar at Penn for the ATLAS ITk Detector

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The high-luminosity LHC requires a complete overhaul of the ATLAS inner tracker subsystem, including a new silicon-strip charged-particle tracking detector. The HCCStar (Hybrid Controller Chip) is one of three new ASICs for this subsystem. As the interface to multiple binary readout ASICs for the strip detector, the HCCStar buffers and forwards controls signals and trigger and readout requests to them, and serializes their output at 640 MHz. All HCCStars undergo a suite of tests to verify their analog and digital functionality, and large statistics of performance with various operational parameters are collected.

Summary (500 words)

The high-luminosity LHC (HL-LHC) introduces new challenges for the ATLAS detector. Detector subsystems will be upgraded to handle higher radiation levels, stricter timing requirements, faster readout, and finer detector granularity. Part of this upgrade is a new silicon-strip charged-particle detector for the inner tracker subsystem (ITk strips). The HCCStar (Hybrid Controller Chip) is one of three new ITk ASICs (application-specific integrated circuits), which is the interface to the detector analog front-end ASICs, the 256 channel ABCStar (ATLAS Binary Chip). The HCCStar forwards clock and control signals to up to 11 ABCStar ASICs. This control data includes triggers, event data readout requests, register read and write commands, test pulse generation, and resets. ABCStar event data, as well as register read data, are sent back to the HCCStar at 160Mbps. The HCCStar combines data for the same event from all inputs and sends out this combined data at 640 Mbps.

The ITk strips upgrade will require approximately 25,500 HCCStars. Pre-production ASICs are manufactured on mixed silicon wafers containing 557 HCCStars, so roughly 50 wafers will be needed for production. Using a wafer probing station and a custom designed probe card, contact can be made with all input and output pads of an individual HCCStar die on a wafer and their digital and analog functionality can be tested. Based on the results of these tests, the wafers are diced and passing die are distributed for detector assembly.

Yield of passing die is above 90% after probe testing, exceeding expectations. Analog functionality tests include ensuring that the onboard voltage regulator can achieve 80 mV above and below the working point voltage of 1.2V for future adjustment, calibrating the onboard ADC and using it for remote monitoring to ensure that currents and communication line levels are within expected ranges. The trigger test checks that the HCCStar receives and distributes trigger requests correctly, and correctly receives and identifies errors in simulated ABC readback. The memory test involves setting and reading registers and memory on the HCCStar and on simulated ABCStars, checking their default values after resets, and ensuring that malformed commands are ignored. The passthrough test checks that the HCCStar correctly interprets and reformats control messages to send to individual ABCStars. Since the HCCStar is designed for a high-radiation environment, large portions of its logic and clock signals are triplicated to provide triple modular redundancy of vital operational logic and programmable register settings. The triplicated clocks test disables individual triplicated clock signals and reruns a critical subset of the trigger and memory tests, to ensure that the individual paths of the triplicated logic work correctly.

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