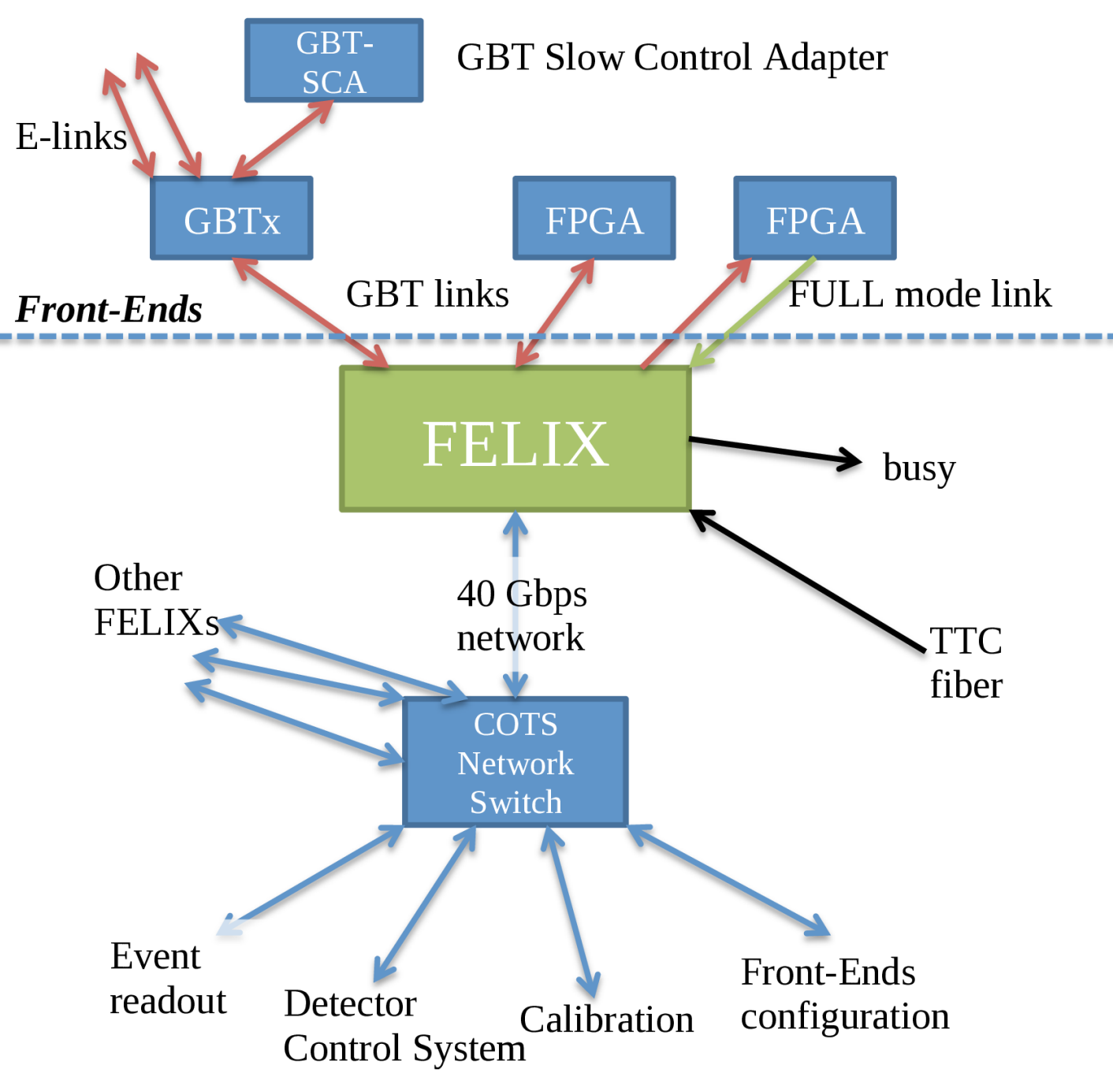
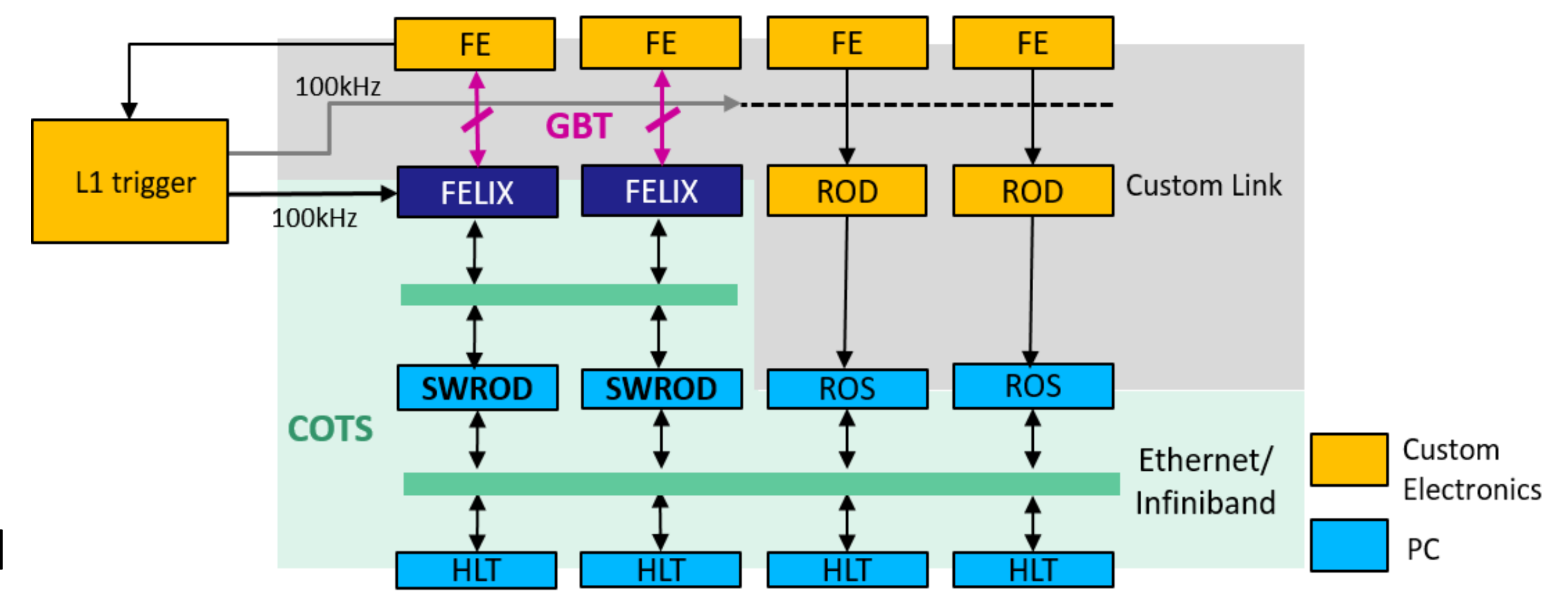


Introduction

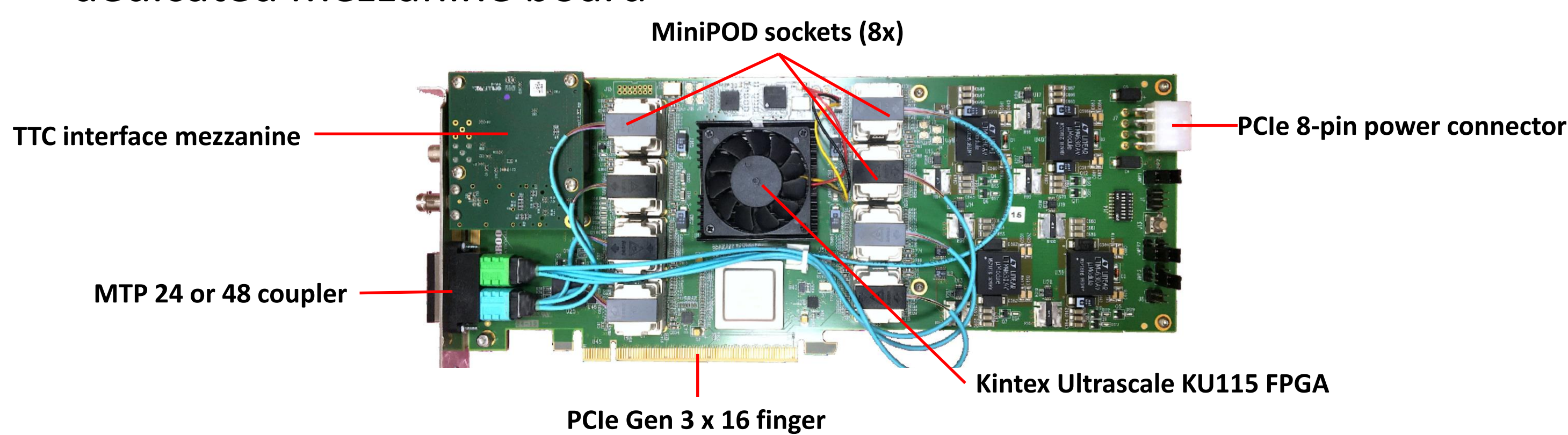


- FELIX: Front-End Link eXchange
- ATLAS-wide effort to harmonise detector readout systems.
- Interface between the optical links of the on-detector electronics and commercial Ethernet
- Components:
 - Custom FPGA interface card (FELIX card)
 - Commercial 25/100 GbE network card (NIC)
 - Commodity server
- First generation FELIX cards are already used by some sub-detectors in Run 3 (2022 – 2026):
 - 105 FELIX cards in 64 servers
- Starting with HL-LHC in Run 4 (2028 onwards) used ATLAS-wide:
 - more than 500 cards in 250+ servers



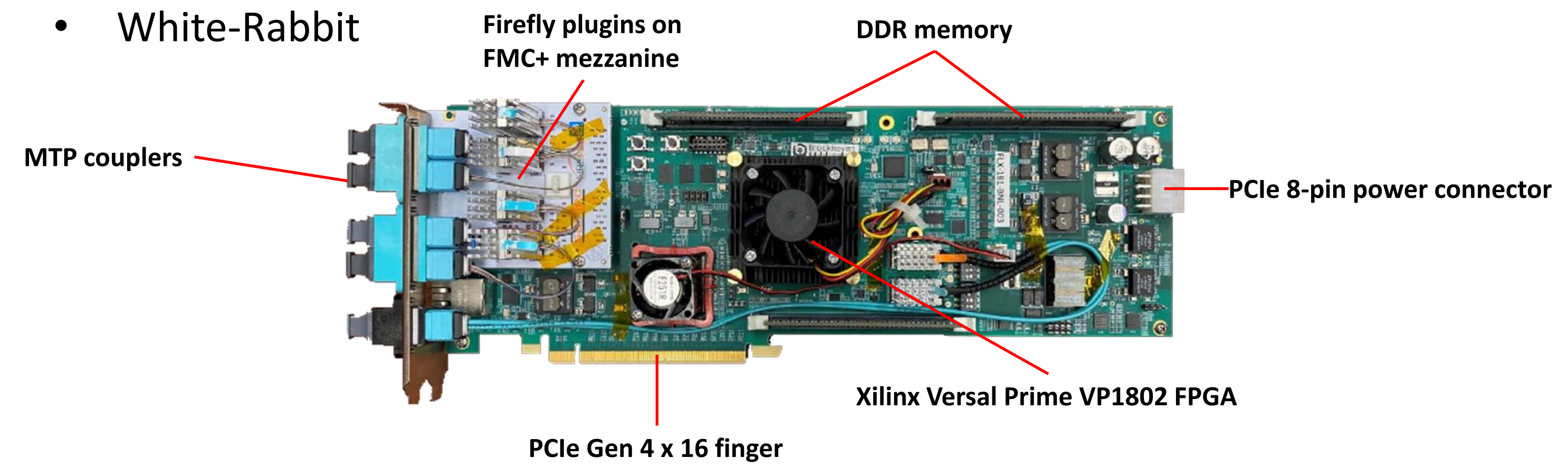
Hardware for Run 3 (FLX-712)

- PCIe-based FPGA card with Xilinx Kintex Ultrascale KU115
- 8 MiniPOD plugins provide up to 48 bidirectional optical links (*most common version have 4 MiniPODs mounted, i.e. 24 links*)
- PCIe 3.0 interface with 16 lanes giving a bandwidth of 128 Gb/s
- FPGA firmware implements two identical endpoints with 8 lanes
- Connection to host CPU through on-board PEX PCIe switch
- Interface to ATLAS Timing, Trigger and Control (TTC) systems through dedicated mezzanine board



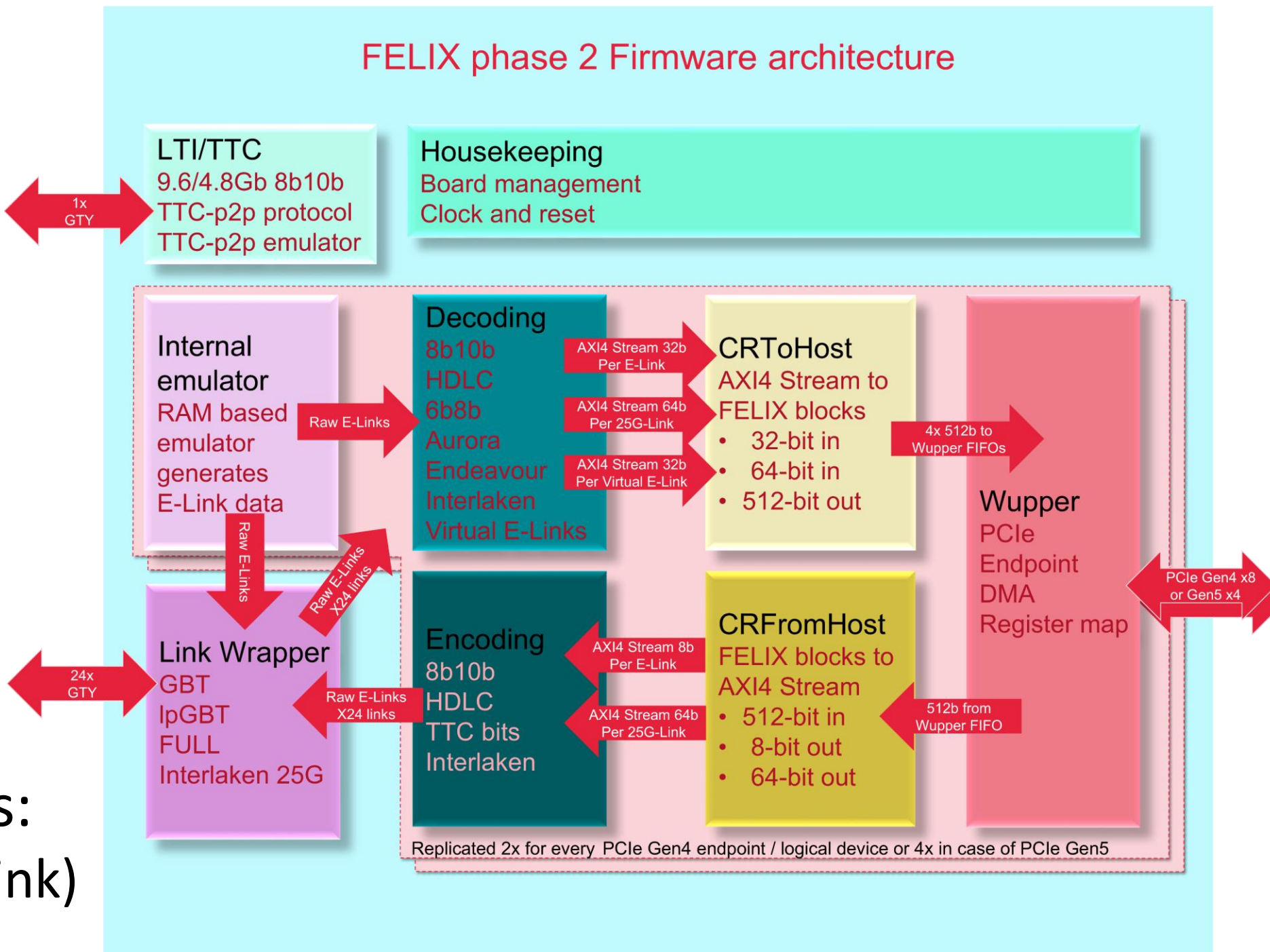
Prototyping hardware for Run 4 (FLX-181)

- Based on new Xilinx Versal Prime VP1802 FPGA
- Also evaluating Versal Premium and Virtex Ultrascale+ FPGAs.
- 24 optical links (Samtec Firefly) with up to 25 Gb/s
- PCIe 4.0 x 16 interface providing 256 Gb/s of bandwidth to the host (possibility to use PCIe 5.0 with Versal Premium FPGAs)
- New TTC interfaces supported:
 - ATLAS Phase-II TTC point-to-point
 - White-Rabbit



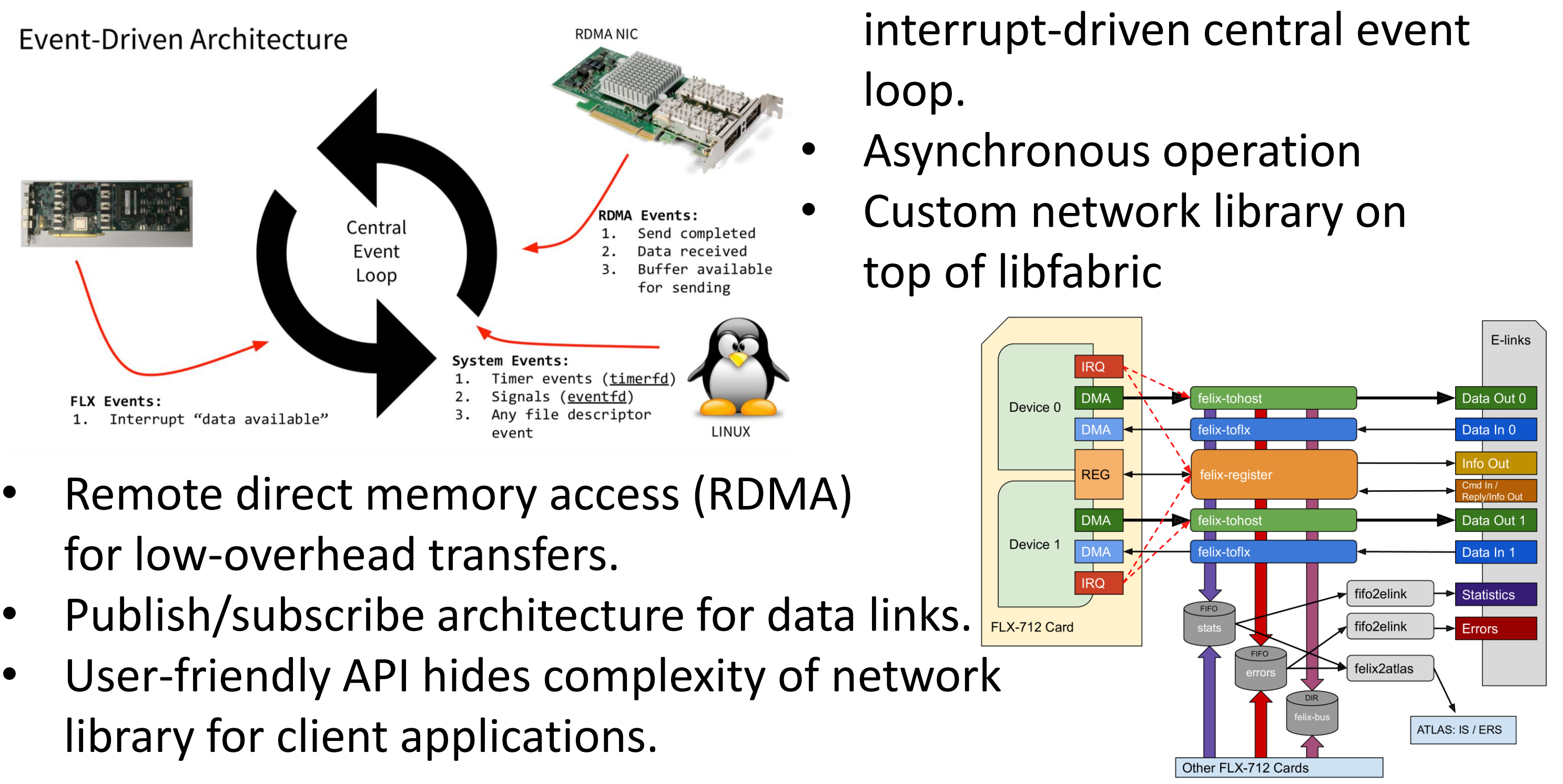
FPGA firmware

- Unified firmware for all hardware variants with same top-level entity.
- Customisation via parameters during synthesis.
- Modular structure for sending / receiving data paths with AXI-Streaming interface.
- Various firmware flavours:
 - GBTx (4.8 Gb/s detector link)
 - IpGBT (5.12/10.24 Gb/s)
 - FULL mode (9.6 Gb/s FPGA link)
 - ITk Pixel (10.24 Gb/s) & Strips
 - LTDB
 - Interlaken (25 Gb/s link)
 - ...
- Using Universal VHDL Verification Methodology (UVVM) framework as part of a Continuous Integration (CI) workflow for development



Readout software (Run 3 and Run 4)

- Readout software consists of an interrupt-driven central event loop.
- Asynchronous operation
- Custom network library on top of libfabric
- Remote direct memory access (RDMA) for low-overhead transfers.
- Publish/subscribe architecture for data links.
- User-friendly API hides complexity of network library for client applications.



Commissioning for Run 3

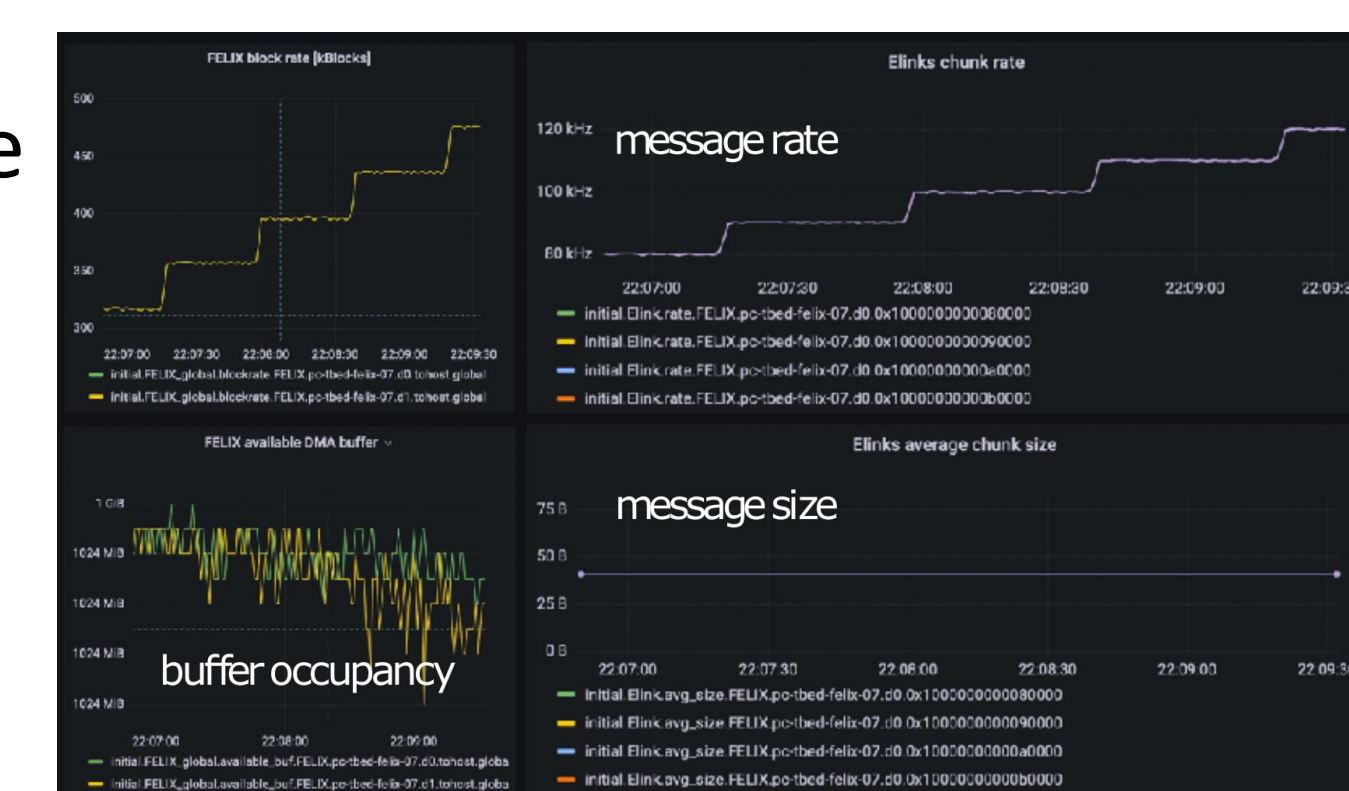
- FELIX is used by subdetectors starting with Run 3:
 - New Small Wheel (NSW)
 - Liquid Argon (LAR)
 - BIS78
 - L1Calo

Host	fix-init	feconf	felix-tohost	register	felix2atlas
ATCN-only links	e0	d0	d1	d0	d1
pc-tdq-fix-1tc-felix-00	DONE	DONE	DONE	RUNNING	RUNNING
pc-tdq-fix-1tc-gfex-00	DONE	DONE	DONE	RUNNING	RUNNING
pc-tdq-fix-1tc-jfex-00	DONE	DONE	DONE	RUNNING	RUNNING
pc-tdq-fix-1tc-trex-00	DONE	DONE	DONE	RUNNING	RUNNING
pc-tdq-fix-1tc-trex-01	DONE	DONE	DONE	RUNNING	RUNNING

- Application control and monitoring with Supervisor
 - Starting & restarting of DAQ applications
 - Monitoring & control through web-interface

- Monitoring integrated into ATLAS-wide infrastructure:

- Visualisation of FELIX readout application through graphical web-interface.
- Integration into ATLAS-wide Error Reporting System (ERS)
- Performance of FELIX machines and network equipment is recorded by computer-cluster monitoring



Outlook and on-going developments for HL-LHC (Run 4)

- **1 MHz readout**
 - Run 3 readout rates can be increased by adding additional DMA paths in firmware.
 - System was stress-tested with Run 4 trigger rates (1 MHz)
- **ITk integration**
 - FELIX also in use by ITk Pixel and Strips during production and testing

