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FELIX: the new ATLAS readout system from Run 3 to High Luminosity LHC

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The Front-End Link eXchange (FELIX) system is a new ATLAS DAQ component designed to meet the evolving needs of detector readout into the High-Luminosity LHC era. FELIX acts as the interface between the data acquisition; detector and trigger timing and systems; and new or updated trigger and detector front-end electronics. FELIX routes data between custom serial links from front-end electronics to data collection and processing components via a commodity switched network. This presentation covers the design of FELIX and its evolution for High-Luminosity LHC, plus commissioning activities ahead of Run 3.

Summary (500 words)

In the decade leading up to the High-Luminosity LHC programme, the collider will deliver significantly increasing instantaneous luminosities to experiments such at ATLAS. Alongside the luminosity increase, the number of collisions per beam crossing will also rise, resulting in larger and more complex events for the Trigger and Data Acquisition (DAQ) systems to process. The Front-End Link eXchange (FELIX) system has been developed to meet ATLAS' DAQ needs in this evolving environment. A key goal of this upgrade is to improve the capacity, flexibility and scalability of the detector readout system while also providing a single common platform for all detector components.

FELIX acts as the interface between the data acquisition; detector control and TTC (Timing, Trigger and Control) systems; and new or updated trigger and detector front-end electronics. The system functions as a router between custom serial links from front end ASICs and FPGAs to data collection and processing components via a commodity switched network. The serial links may aggregate many slower links or be a single high bandwidth link. FELIX also forwards the LHC bunch-crossing clock, fixed latency trigger accepts and resets received from the TTC system to front-end electronics. FELIX is being commissioned for a subset of ATLAS detector components ahead of LHC Run 3, before being rolled out for the rest of ATLAS in time for Run 4, the start of the High-Luminosity LHC era.
FELIX uses commodity server technology in combination with FPGA-based PCIe I/O cards to receive data from detector and trigger components. Data are passed between the I/O cards and host server via multiple DMA channels. The servers hosting the cards then run a software routing platform which both serves and receives data to and from network peers.

Commodity servers connected to FELIX systems via the same network run the new multi-threaded Software Readout Driver (SW ROD) infrastructure for event fragment building, buffering and detector-specific processing to facilitate online selection.
Ahead of High-Luminosity LHC the FELIX system will be upgraded to support higher trigger rates and data volumes, as well as the processing and detector control requirements of the new ATLAS components planned for this time. This includes support for the new lpGBT link protocol, as well as an Interlaken-based 25 Gb/s standard for selected systems. Some time-critical detector control processes (such as those required to operate the new ATLAS Inner Tracker (ITk)) will also be supported with the FELIX firmware (current Run 4 design shown in supporting figures).

This presentation will cover the design of FELIX, as well as its planned evolution for High Luminosity LHC. The results of commissioning activities ahead of Run 3 will be presented, alongside those from ongoing High-

Luminosity LHC demonstrator programmes and performance benchmarks using Run 3 hardware at Run 4 rates.

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