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LTDB, the Lar Trigger Digitizer Board: from design to mass production for ATLAS Liquid Argon Calorimeters Phase-1 Upgrade

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To increase granularity, resolution, and provide longitudinal shower shape information from the ATLAS LAr calorimeters to its level-1 trigger processor, a new radiation-hard board has been designed during the phase-1 upgrade. This Lar Trigger Digitizer Board adapts and digitizes up to 320 detector inputs using custom ADCs and sends the serialized data through 200Gbps optical links. The run control of the board is implemented through five bidirectional GBT links. 150 boards have been produced and validated with an elaborated test-bench based on a complex custom-built signal injector and the FELIX DAQ. The board architecture and the test-bench organization are presented.

Summary (500 words)

ATLAS Liquid Argon (Lar) Calorimeters provide key inputs to the ATLAS trigger system. With the luminosity upgrade of the LHC during the Run 3 and beyond, a more efficient event-selection mechanism is required. The motivation of the Phase 1 upgrade was to enhance the granularity and resolution of the Lar Calorimeters and provide additional longitudinal shower shape information to the Level-1 trigger processor. The 6000 legacy "trigger towers"have been divided into 34000 finer cells, called "Super Cells". This new scheme represents about a ten-fold increase of information. To cope with this higher data rate, the Super Cells are digitized on a new board, the Liquid Argon Trigger Digitizer board (LTDB) before being sent to the level-1 trigger processor.

The LTDB is a mixed analog-digital board. The analog stage receives up to 320 input channels. In order to take advantage of the full dynamic range of the digitizer, the pedestal and gain of each ADC driver is adapted depending on the geographical region of the super cell in the calorimeters. To optimize manufacturing costs, a generic layout has been designed allowing the channel configuration through a set of few resistors. About 200 different configurations have been implemented on 7 board flavors. The analog stage also outputs up to 64 summed signals to the tower builder board, the analog legacy trigger, each of the signal being the sum of 4 super cells. The digital stage digitizes the conditioned detector signals at 40 MHz using quad-channel 12-bits NEVIS ADC. The ADC outputs are serialized through a dual-channel LOCx2 ASICs at 5.12Gbps per channel. The optical conversion is performed through low profile (6.4mm) Miniature Optical Transmitters (MTx). Up to 40 optical fibers organized in 4 MTP assemblies carry the data out to the level-1 trigger processor. The control and monitoring of LTDB is realized via 5 bidirectional GBT links connected to the Front-End LInks eXchange (FELIX) boards in ATLAS TDAQ system. FELIX distributes the TTC (Time, Trigger and Control) clock and BCR (Bunch Counter Reset) signal via down-links to the LTDB. FELIX also controls 5 GBTx and all ASICs via the 5 GBT SCA (Slow Control Adapter) on the LTDB. Power supplies are distributed through a Power Distribution mezzanine Board. Every active COTS component and ASIC has been qualified against the ATLAS Phase 1 radiation tolerance requirements.

An LTDB represents about 13000 components embedded on a 24-layers, 41x49cm2 wide, PCB cooled by water circulation through cooling plates. 150 boards, manufactured by two sub-contractors, have been fully validated and integrated in lab using a specific test stand based on a complex custom-built signal injector, the STM (Saclay Test Module) board, an ad-hoc FELIX DAQ firmware and python-based GUI and scripts for test routine automation. By injecting arbitrary waveforms (DC level, Lar Pulse signals, Ramp, Sinewave) the STM

was essential to verify the noise, linearity, gain, peaking time and distortion of each LTDB channel as well as the LTDB fiber mapping.

This contribution presents the LTDB design, the STM architecture and the test stand organization.

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