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Qualification tests of the PASTTREC readout ASIC for straw tube detectors

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PASTTREC is an 8-channel readout ASIC for the Straw Tube Tracker (STT) and the Forward Tracker (FT) detectors in the PANDA and for the Straw Tracking System (STS) in the HADES experiments, both at the FAIR facility. Since more than 1500 ASICs were produced for both experiments, efficient qualification tests are required. For this purpose, the multi-chip test setup and dedicated verification procedures were developed. In this contribution, the results for the first batch of 280 PASTTRECs, showing a yield of approximately 94%, with a particular emphasis on the process-related spread of key ASIC parameters, will be discussed.

Summary (500 words)

PASTTREC is an 8-channel ASIC developed for a binary readout of gaseous straw tube detectors. Such a readout requires fast shaping and ion tail cancellation with baseline stabilization, followed by discriminator with binary output. The ASIC was developed for the Straw Tube Tracker (STT) and the Forward Tracker (FT) in the PANDA experiment and for the Straw Tracking System (STS) in the HADES experiment, both at the FAIR facility. In these tracking systems, detectors are built of modules, each one containing 32 straws read out by two dedicated Front-End Boards (FEBs), each one hosting two PASTTRECs. The 16-channel FEB is the main objective of the mass tests.

PASTTREC provides variable gain (four predefined settings: 0.67 mV/fC, 1 mV/fC, 2 mV/fC and 4 mV/fC), variable peaking time (four predefined settings with measured peaking time in the range 25-67 ns) and tail cancellation with variable time constants. Due to the large number of possible settings, only five default configurations, useful from the experiments point of view, were selected for tests. A test system, measuring up to eight FEBs (16 PASTTRECs) in parallel, was developed together with a dedicated procedures for baseline, gain, and noise measurement. The setup allows not only to verify PASTTREC performance, but also to optimize ASICs settings. Additionally, the calibration of a Time-over-Threshold (ToT) measurement, performed by an external Time-to-Digital Converter (TDC), can be obtained to improve charge deposition estimation.

The first tests were conducted in 2021 for production batch of 280 PASTTRECs (140 FEBs) in total. The main goal of the tests, with the large number of ASICs, was to understand the process-related spread of parameters and to find the optimal ASIC settings for the experiments. Furthermore, additional tests were performed on a few boards with the setup comprising straw tubes and an X-ray source, to verify the operation of the complete detector readout chain.

As a result of the tests, 15 ASICs out of 280 were marked as “not good”. Seven were found non-compliant due to communication problems or too large baseline offset, and eight more with too large gain spread. These eight chips will be left as an optional backup. Finally, approximately 94% of the PASTTRECs were considered compliant. All of these chips were characterized with baseline, gain, noise, and ToT measurements. Since PASTTREC has binary output, the baseline measurement was performed first, and the baseline correction, applied by the 5-bit DAC placed in each channel, was determined. This correction was practically the same for all tested chip configurations. Next, the remaining parameters were measured. As expected, smaller noise was measured for higher gain settings, reaching about 1000 electrons at the highest gain, suggesting that higher gain settings would be used in the experiment.

In this contribution, an overview of the test setup and procedures, together with the results for the batch of 280 PASTTRECs will be discussed, with particular emphasis on process-related spread of key parameters.

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