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Electronics for the far-forward CMS muon detector upgrade, ME0

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With the High Luminosity upgrade of the LHC we expect increased instantaneous luminosities up to 5x10ˆ34 cmˆ-2sˆ-1, or five times more than the original values. In order to maintain performance of the Compact Muon Solenoid (CMS) experiment under these conditions, ME0 is one of the three new muon sub-detectors. The readout electronics for ME0 must be designed to accommodate high data rates and be sufficiently radiation hard to operate close to the beamline. The design and development status of the readout electronics for ME0 will be presented, along with recent results from integration tests performed using the first prototypes.

Summary (500 words)

The ME0 muon detector in the Compact Muon Solenoid (CMS) experiment is one of the three new muon detectors, alongside GE1/1 and GE2/1, being added based on the triple Gas Electron Multiplier (GEM) technology. Since the Large Hadron Collider (LHC) is expected to deliver instantaneous luminosities five times more than the original design value in the high luminosity era, these upgrades for the muon system are necessary to maintain their performance under these new challenging conditions. The ME0 detector, which is the closest one to the beamline among the three, is designed to cover the forward region of 2.0<|η|<2.8, thus supplementing the forward muon system with additional hits between 2.0<|η|<2.4 and also extending the acceptance of the forward muon detectors for the first time to |η|=2.8.

The ME0 detector will be made out of 36 modules, with 18 modules in each endcap, arranged in a wide planar ring, centered on the beamline. Each module consists of a 6-layer triple GEM stack covering an azimuthal angle of 20 degrees. Being located so close to the beamline, the readout electronics for ME0 must be designed to deal with high data rates and be sufficiently radiation hard. The signal from the Readout Board (ROB), which is segmented in radial strips for each η partition, on the GEM chambers are readout by VFAT3b Application Specific Integrated Circuits (ASICs). The GEM Electronic Board (GEB) which is placed on top of the ROB hosts the VFAT3b ASICs and is responsible for routing the signals from them to the Optohybrid (OH) board, also connected to the GEB. Unlike GE1/1 and GE2/1, the ME0 OH has been designed to operate without an FPGA in order to ensure radiation hardness. It will use the radiation-hard CERN designed Low Power Giga Bit Transceiver (lpGBT) ASIC and the Versatile Link+ Transceiver (VTRx+) for high bandwidth optical links at 10.24 Gb/s to transmit data back to the backend electronics without any compression, therefore providing the benefit of high data rates. The backend system for ME0 will be based on the ATCA standard.

The first prototypes for the different electronic components have been produced and are undergoing extensive testing at different teststands across several institutions. Fig. 1d shows the integration of the front-end electronics at one such teststand, including the GEB, OH and the VFAT3b ASICs. The testing procedure has been designed to establish communication between the different components, calibrate them and determine the noise in the system. The design of the readout electronics for ME0 will be described in the talk, including the development status of the first prototypes along with recent results from the integration testing.

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