Clock stability measurements using the Barrel Calorimeter Processor V1 (BCP-V1)

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- for the CMS collaboration -

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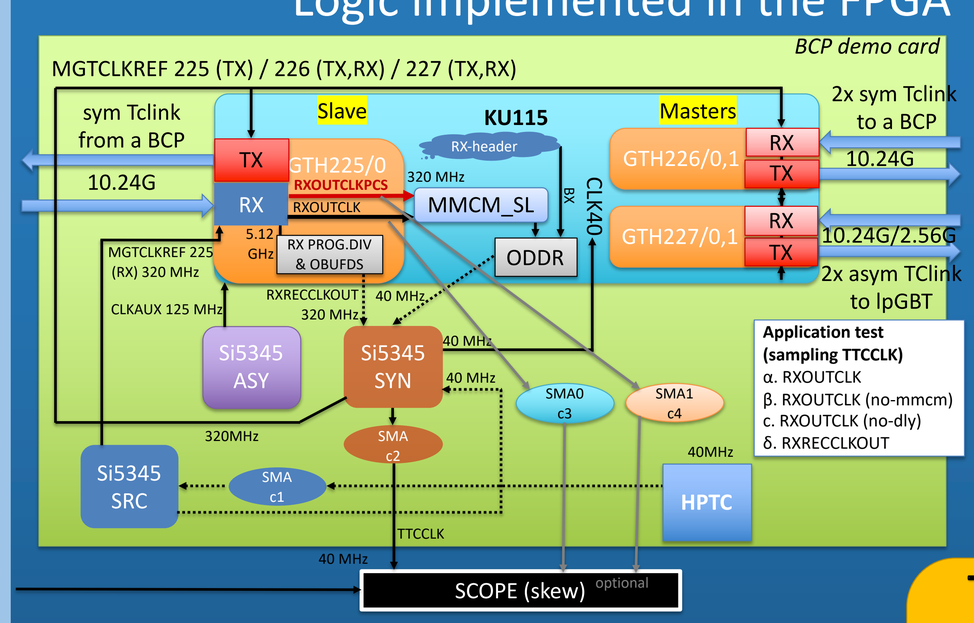
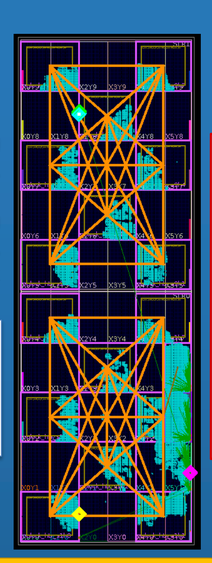
Logic implemented in the FPGA

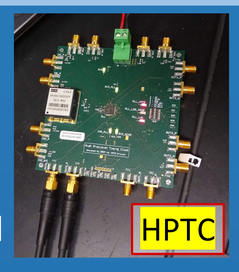




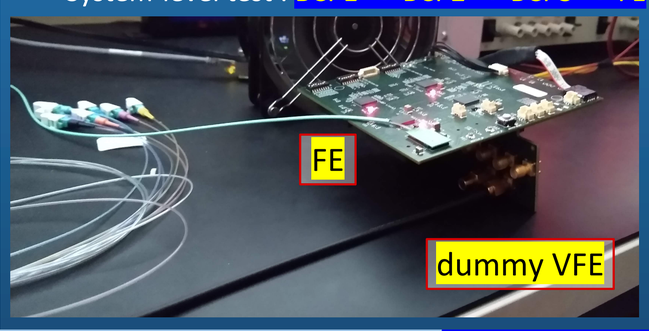
- ZYNQ-FPGA interface : Fast control and configuration (2-3 sec) times
- Implementing CERN's Timing Compensation links [1] (TClinks rev1.4)
- Evaluating different clock paths using BCP-V1 [2]±
- Implementing heaters [3] (controlling the temperature of the FPGA)

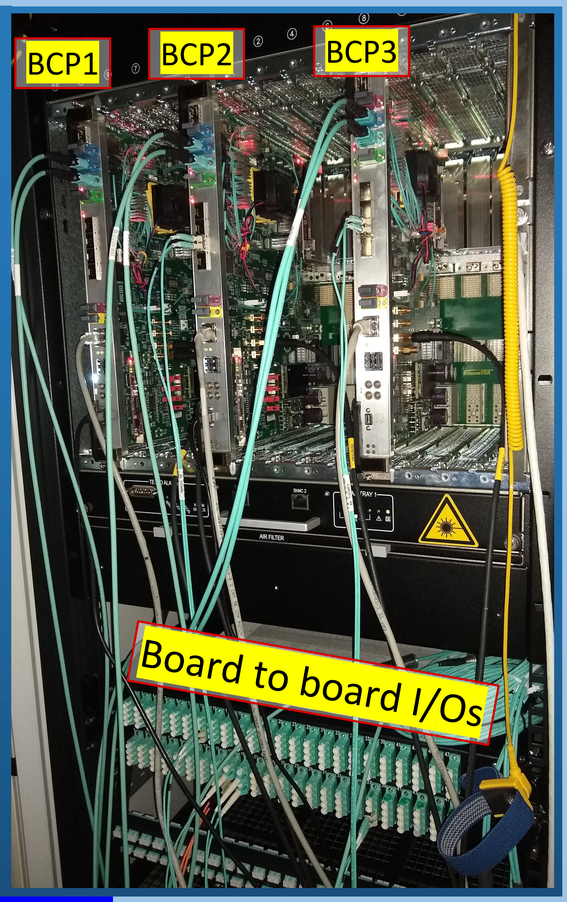
Thanks to C. Borca (INFN Torino) automating the scope

SETUP

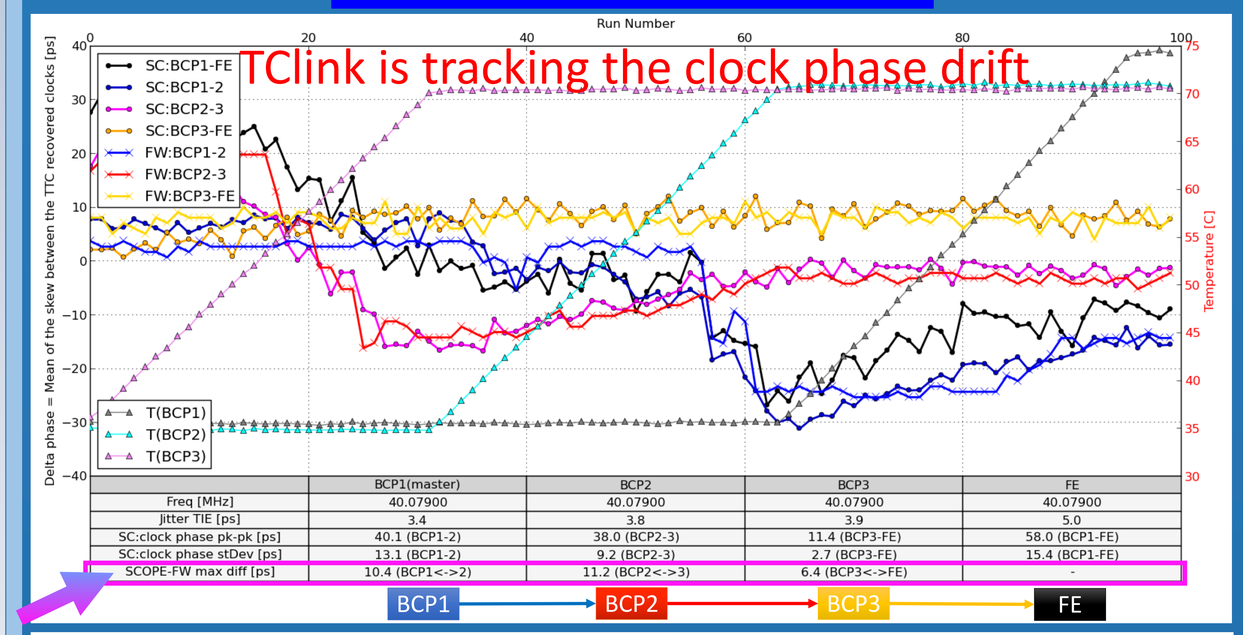


- 3x BCPs in an ATCA crate
- MPO/LC patch panel
- CMS-ECAL Front-End (FE) [4]
- Dummy Very- Front-End (VFE) used to sample the recovered clock
- High-Precision Timing Clock generator (HPTC)
- Oscilloscope : Teledyne's LabMaster (36GHz)
- Application-level test : BCP1 → BCP2
- System-level test : BCP1 → BCP2 → BCP3 → FE



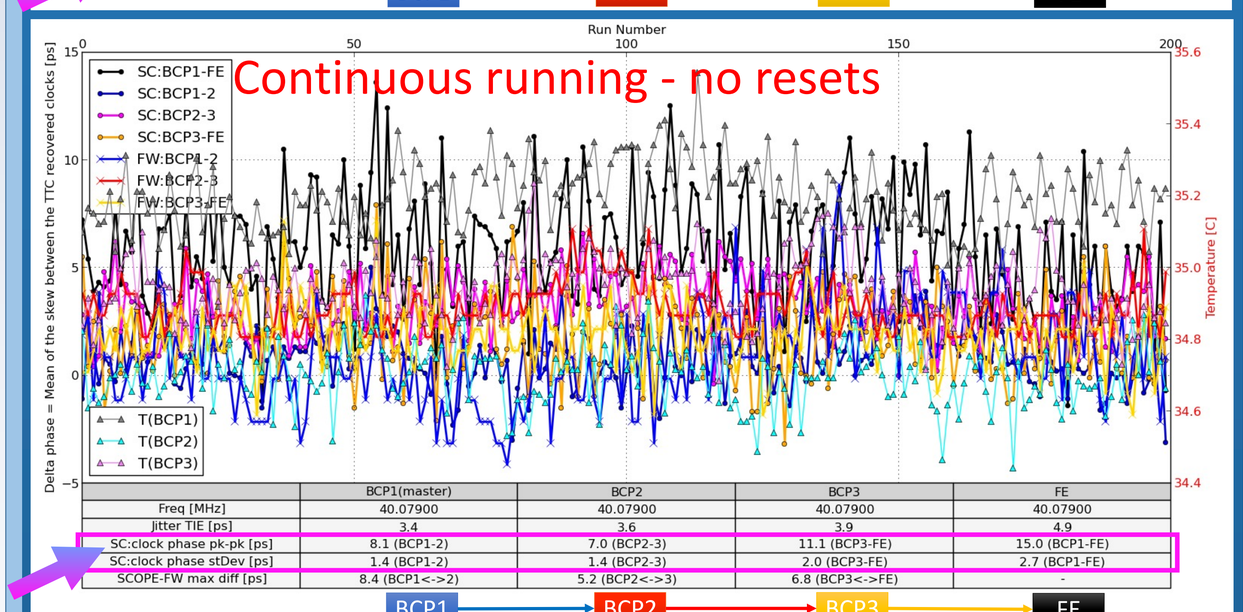


BCP1 → BCP2 → BCP3 → FE



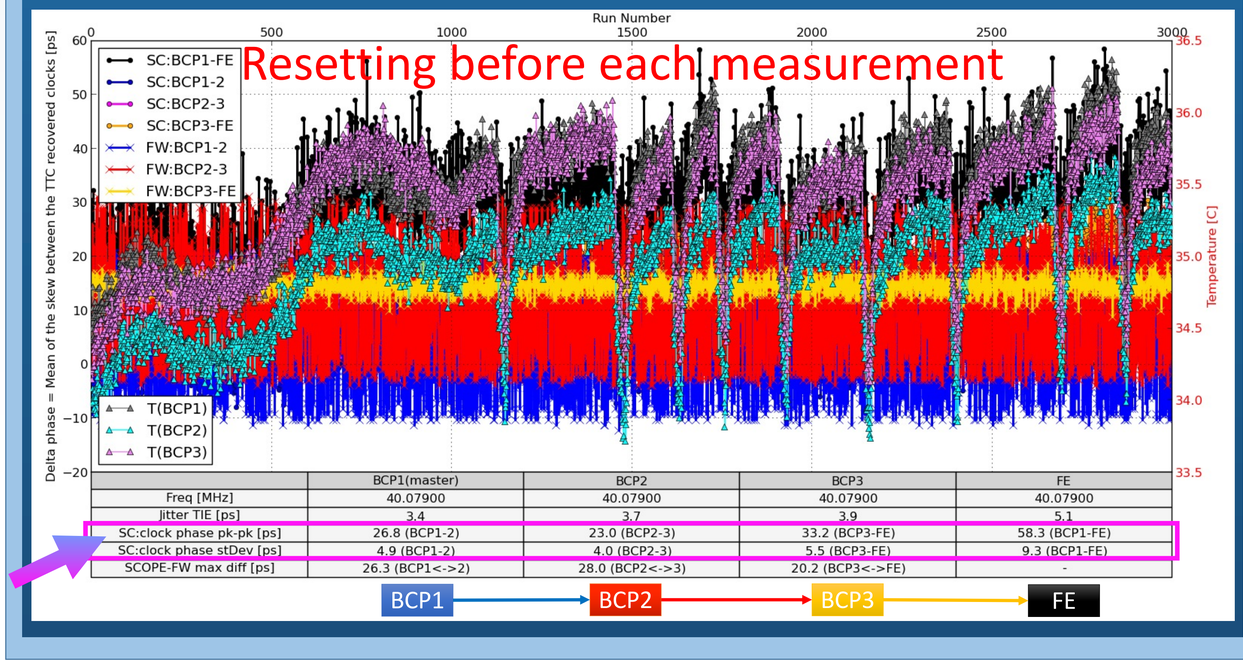
	BCP1(master)	BCP2	BCP3	FE
Freq [MHz]	40.07900	40.07900	40.07900	40.07900
Jitter TIE [ps]	3.4	3.8	3.9	5.0
SC:clock phase pk-pk [ps]	40.1 (BCP1-2)	38.0 (BCP2-3)	11.4 (BCP3-FE)	58.0 (BCP1-FE)
SC:clock phase stDev [ps]	13.1 (BCP1-2)	9.2 (BCP2-3)	2.7 (BCP3-FE)	15.4 (BCP1-FE)
SCOPE-FW max diff [ps]	10.4 (BCP1<->2)	11.2 (BCP2<->3)	6.4 (BCP3<->FE)	-

BCP1 → BCP2 → BCP3 → FE



	BCP1(master)	BCP2	BCP3	FE
Freq [MHz]	40.07900	40.07900	40.07900	40.07900
Jitter TIE [ps]	3.4	3.6	3.9	4.9
SC:clock phase pk-pk [ps]	8.1 (BCP1-2)	7.0 (BCP2-3)	11.1 (BCP3-FE)	15.0 (BCP1-FE)
SC:clock phase stDev [ps]	1.4 (BCP1-2)	1.4 (BCP2-3)	2.0 (BCP3-FE)	2.7 (BCP1-FE)
SCOPE-FW max diff [ps]	8.4 (BCP1<->2)	5.2 (BCP2<->3)	6.8 (BCP3<->FE)	-

BCP1 → BCP2 → BCP3 → FE

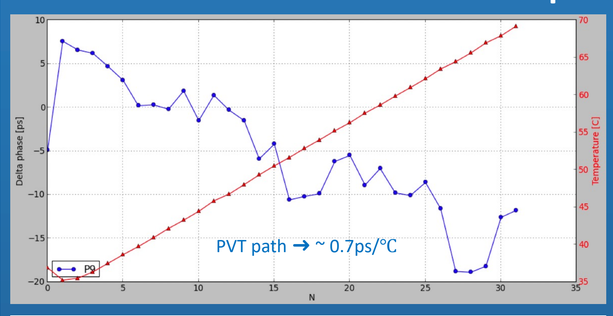


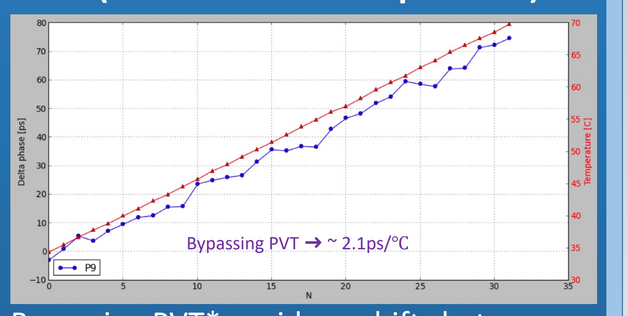
	BCP1(master)	BCP2	BCP3	FE
Freq [MHz]	40.07900	40.07900	40.07900	40.07900
Jitter TIE [ps]	3.4	3.7	3.9	5.1
SC:clock phase pk-pk [ps]	26.8 (BCP1-2)	23.0 (BCP2-3)	33.2 (BCP3-FE)	58.3 (BCP1-FE)
SC:clock phase stDev [ps]	4.9 (BCP1-2)	4.0 (BCP2-3)	5.5 (BCP3-FE)	9.3 (BCP1-FE)
SCOPE-FW max diff [ps]	26.3 (BCP1<->2)	28.0 (BCP2<->3)	20.2 (BCP3<->FE)	-

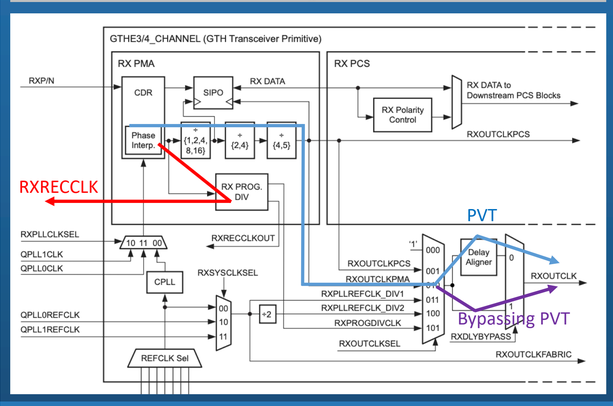
BCP1 → BCP2 → BCP3 → FE

BCP1 → BCP2

Evaluating the impact of the temperature in the FPGA with the clock phase (varies clock paths)

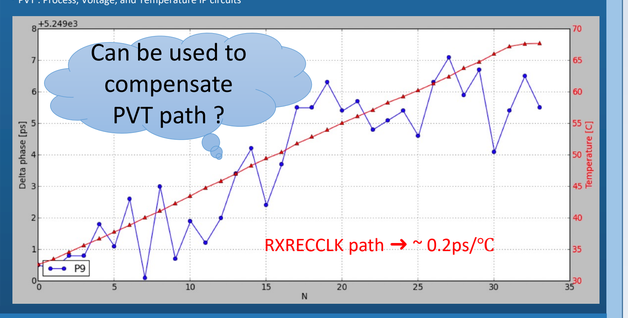




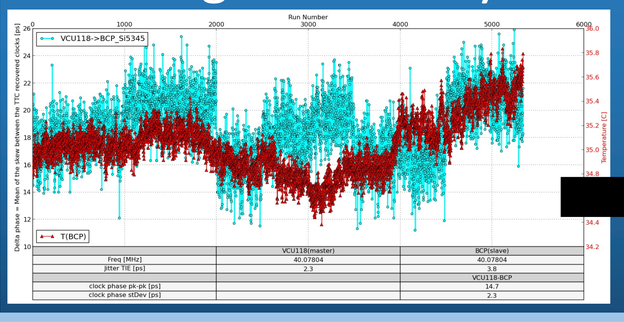


Bypassing PVT* avoids ps shifts between resets but has strong temperature variation

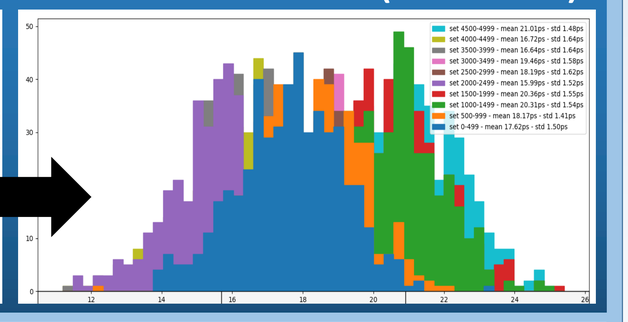
* PVT : Process, Voltage, and Temperature IP circuits



Resetting once every 500 measurements (via PVT)



	VCU118(master)	BCP(slave)
Freq [MHz]	40.07804	40.07804
Jitter TIE [ps]	2.3	3.8
clock phase pk-pk [ps]	VCU118-BCP	14.7
clock phase stDev [ps]		2.3



Conclusions

✓The TClink calculated phase drift is ± ~11 ps of the scope measured phase drift

✓Each reset can cause an offset (~4 ps max) on the phase clock distribution when going through the Transceiver's Delay aligner (PVT)

✓When bypassing the PVT, the phase of the clock significantly varies with temperature

✓The clock distribution of one full branch of the future phase 2 upgrade CMS - ECAL Barrel has been emulated. The result σ = 9.3 ps meets the TDR specification [5]

References

[1] TCLink: A Timing Compensated High-Speed Optical Link for the HL-LHC experiments, TWEPP2019
[2] The CMS Barrel Calorimeter Processor demonstrator (BCPv1) board evaluation
[3] A. Agne et al., Seven Recipes for Setting Your FPGA on Fire - A Cookbook on Heat Generators, Microprocessors and Microsystems
[4] CMS ECAL Upgrade Front End card: design and prototype test results
[5] The Phase-2 Upgrade of the CMS Barrel Calorimeters - Technical Design Report (TDR), page 79, section 3.7.1.