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Clock stability measurements using the Barrel Calorimeter Processor V1

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The stability of the clock distributed by the first version of the Barrel Calorimeter Processor (BCP V1) to the front-end electronics has been evaluated and compared with the required performance as specified for the phase 2 upgrade of the CMS Barrel Electromagnetic Calorimeter (EB). The evaluation setup emulated a full clock branch of the planned EB system through multiple stages. The stability of the clock phase and jitter was measured during a long run with no configuration changes as well as many short runs where reconfiguration was applied. Finally, the impact of component temperature variation on the clock was evaluated.

Summary (500 words)

It has been specified that the target performance for the EB upgrade is a clock distribution system with stability lower than 10 ps. This implies that both the jitter and phase stability (skew) must be maintained below this level during transmission across the detector and over long LHC running periods. The baseline clock distribution design embeds the clock within the data which will add some jitter to the recovered clock and may alter its phase. To evaluate this baseline system against the specification, the BCP V1 was used to emulate one branch of the system by cascading three BCP boards in series with one front-end card (BCP1 ⟶ BCP2 ⟶ BCP3 ⟶ FE). The BCP FPGA firmware implemented Timing Compensation (TC) over the links which actively maintained the phase relationship between each stage. The temperature of the FPGA was controlled and monitored by enabling logic heaters in the FPGA in order to estimate the impact of temperature on the clock phase. At the start of each new CMS data run, the FPGA will be reconfigured, the onboard PLLs will be reset and the TC links will be recalibrated which could change the clock phase, so each BCP board in the test was repeatedly controlled to step through this process in order to evaluate any effect on the clock. Results were gathered using a Teledyne Lecroy LabMaster 36 GHz Oscilloscope where the Time Interval Error (TIE) jitter and the phase stability of the clocks were measured. Also, the clock phase stability measurement of the oscilloscope was compared against the estimation calculated by the firmware for each stage of the cascaded system. The advantages and disadvantages of this baseline embedded clock distribution versus a separate, direct clock distribution are also concluded.

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