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A Readout System for Monolithic Pixel Sensor prototypes towards the ITS3 upgrade of the ALICE Inner Tracking System

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The ITS 3 project within the ALICE Experiment is developing an innovative vertex tracker to be installed during the Long Shutdown 3 of the LHC. Based on a commercial 65 nm CMOS imaging technology, it consists of cylindrical sensors that can be installed as close as 18 mm to the interaction point.

In order to validate the technology, test chips were produced in a first submission named MLR1. This contribution will describe the development of a test system for some prototypes of MLR1, namely Analogue and Digital Pixel Test Structures (APTS, DPTS) and pixel matrices with rolling shutter readout (CE65).

Summary (500 words)

The ALICE collaboration is pursuing the development of a novel vertexing detector called ITS3 for the replacement of the three innermost layers of the Inner Tracker System during the Long Shutdown 3 of the LHC.

The new detector will consist of three truly cylindrical layers, with the first layer at a radial distance of 18 mm from the interaction point. This design is enabled by the flexible nature of silicon when thinned down to 20-40 µm. A process called stitching is used to build detector elements up to 300 mm in length, large enough to cover full tracker half-layers with single bent sensors, with the unprecedentedly low material budget of 0.05% X0 per layer.

This technology needs to be verified in terms of radiation hardness and of pixel performance, respectively. MLR1 is first submission in the TowerJazz 65 nm technology and includes a large number of dies in different processing flavours that will provide crucial input into the next design steps.

A portable readout system (Fig. 1) was developed at INFN Cagliari in collaboration with CERN to characterize and test some of the chips in the MLR1 submission, namely:
- APTS, a pixel test structure (4x4 pixels) with analogue readout;
- DPTS a pixel test structure (32x32 pixels) with digital readout;
- CE65, a pixel matrix (different sizes, up to 42x32 pixels) with rolling shutter readout.

The design is meant to be affordable for large-scale distribution to collaborating institutes and retrocompatible with single ALPIDE chips mounted on a carrier board. This contribution discusses the concept, features and performance of the readout system.

The readout system consists of a readout board measuring 108 mm x 100 mm interfaced to a computer via USB 3.0. A PCIe connector accommodates a proximity card that is specific to the chip under test and hosts the needed electronics.

The heart of the system is an ALTERA Cyclone IV FPGA (EP4CE40F23C6N) configurable via a JTAG interface or by an EEPROM. The firmware architecture is shown in Fig. 2. Features include:
- Monitoring the currents provided to the sensor;
- Voltage and current biasing provided by DACs and current sources and sinks in the proximity card;
- For APTS: parallel readout of the 16 analogue pixels up to 4 MSPS and 16-bit resolution;
- For CE65: rolling shutter readout at a user-selectable speed of 10, 20, or 40 MHz and 16-bit resolution.

The readout system is currently being used to conduct comprehensive tests on the prototypes, both in the laboratory and in beam testing facilities –October 2021 at PS, November 2021 at SPS, April 2022 at MAMI, and several planned for the rest of 2022. 50 units of this system were produced and are in the process of being distributed to the collaborating institutes.

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