CMS tracker phase-2 upgrade module noise and mitigation

A Zografos[1], G. Blanchot[1], M. Kovacs[1], S. Maier[2], I. Mateos[1], A. Pauls[3], K. Schleidweiler[1]

[1]CERN, Route de Meyrin, CH-1211 Geneva 23, Switzerland
[2]KIT, Hermann-von-Helmholtz-Platz 1, 76344 Eggenstein-Leopoldshafen, Germany
[3]I. Physikalisches Institut, RWTH Aachen University, Aachen, Germany

1. CMS Phase-2 Outer Tracker Modules

Two module types (2S and PS) will be used in the Compact Muon Solenoid (**CMS**) **Outer Tracker** (OT) **Phase-2 Upgrade** for the High Luminosity Large Hadron Collider (HL-LHC). The 2S modules contain a double strip sensor configuration with an active area of (10×10) cm^2, wire bonded to two front-end hybrids that are powered and controlled by a service hybrid (figure 1). The PS modules contain a strip sensor and a macro-pixel sensor of (5×10) cm^2 wire bonded to two front-end hybrids interconnected with a power hybrid on one side and with an optical readout hybrid on the opposite side (figure 2).
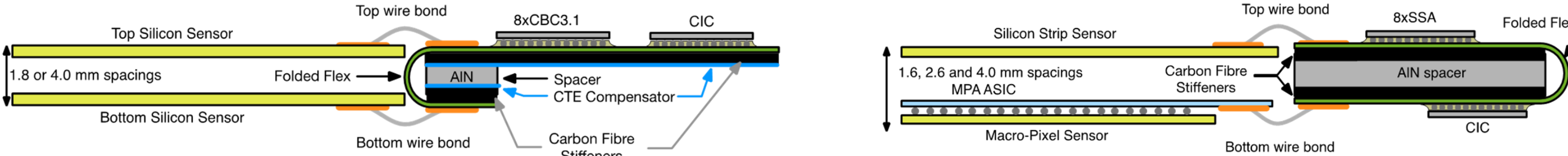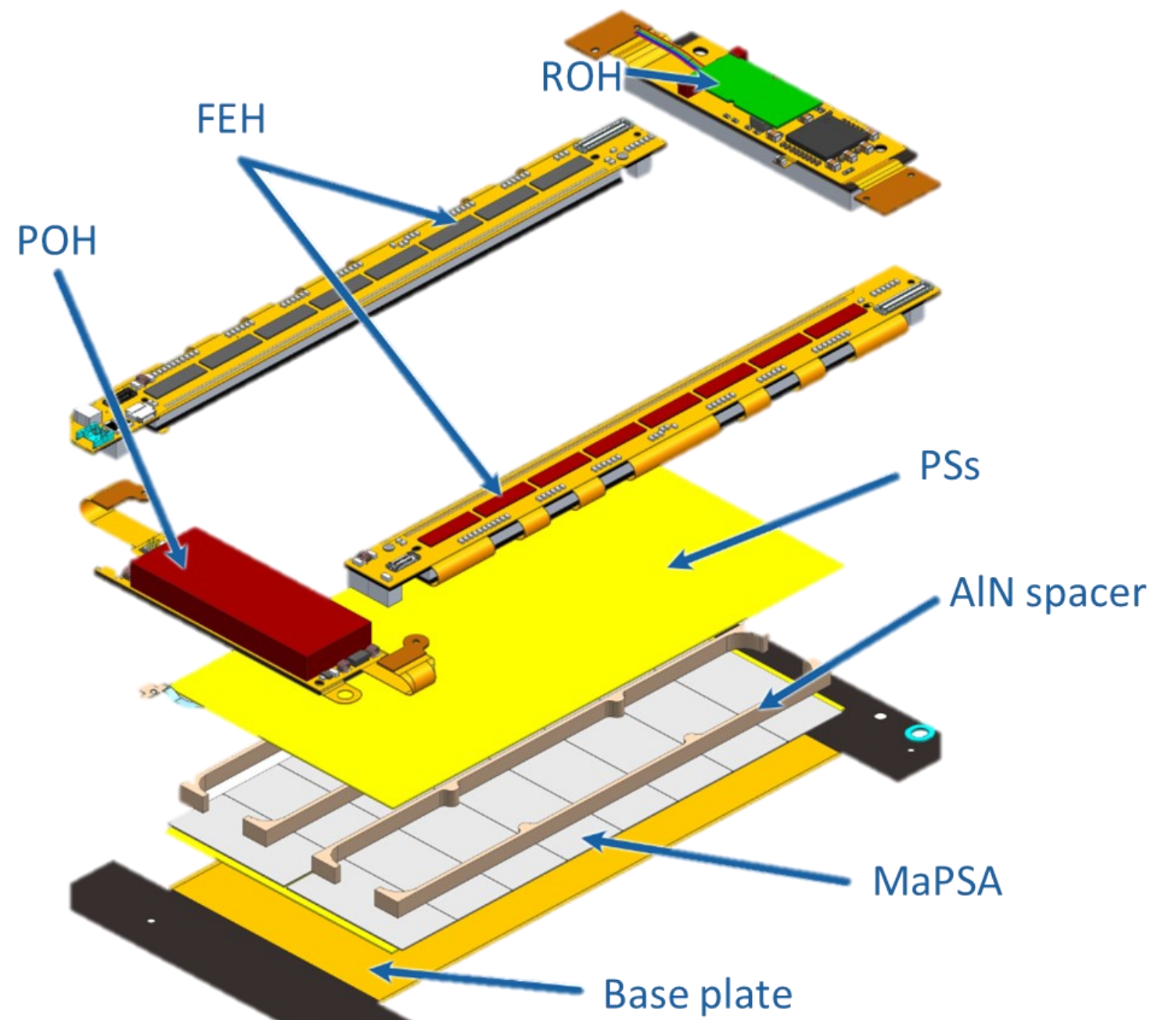

Figure 1: Strip-Strip (2S) module.

Figure 2: Pixel-Strip (PS) module.

2. Problem Description

- The Front-End ASICs of the OT employ binary readout. **Higher noise** means a higher threshold (lower VCth) is needed for the comparator to avoid false hits, and a **higher percentile of signals not being detected**.

- An S curve is acquired by measuring the occupancy (hits per event over a number of events) for different VCth values. The gaussian error function is fit in the data and the σ parameter of the derivative of that function (a gaussian function) is defined to be the noise level (figure 3).

- The **average noise** over all the channels for the PS and the 2S module cases in different prototype modules was measured to be consistently **higher than expected** (figures 4, 5). The yellow lines represent the previous 8CBC3 module prototype and 2SSA board prototype and serve as the baseline for noise for the 2S and PS cases respectively.
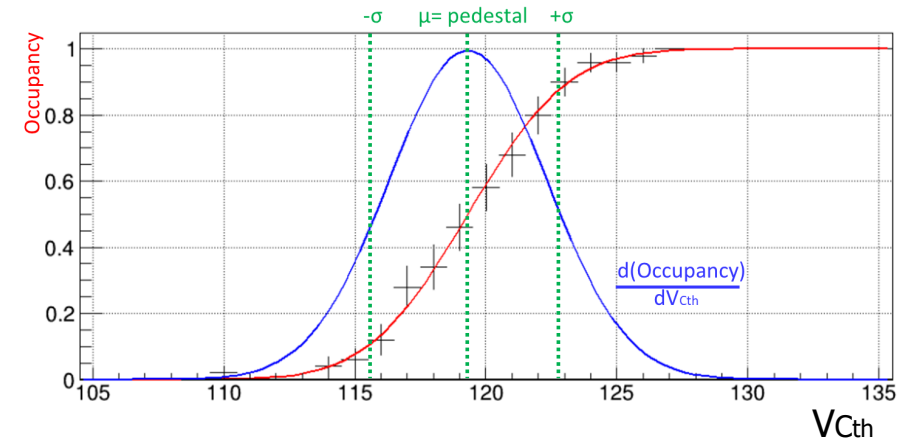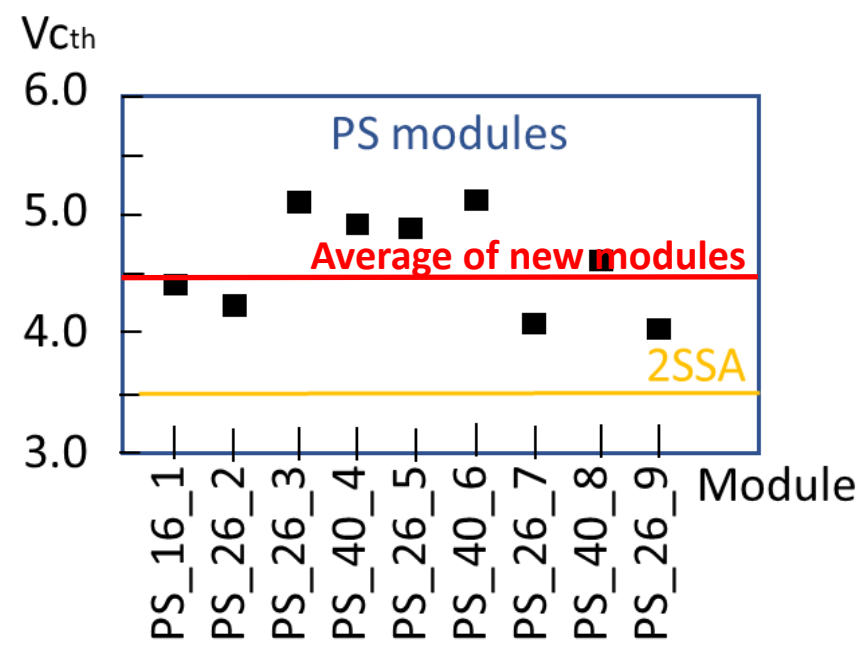

Figure 3: Noise definition.

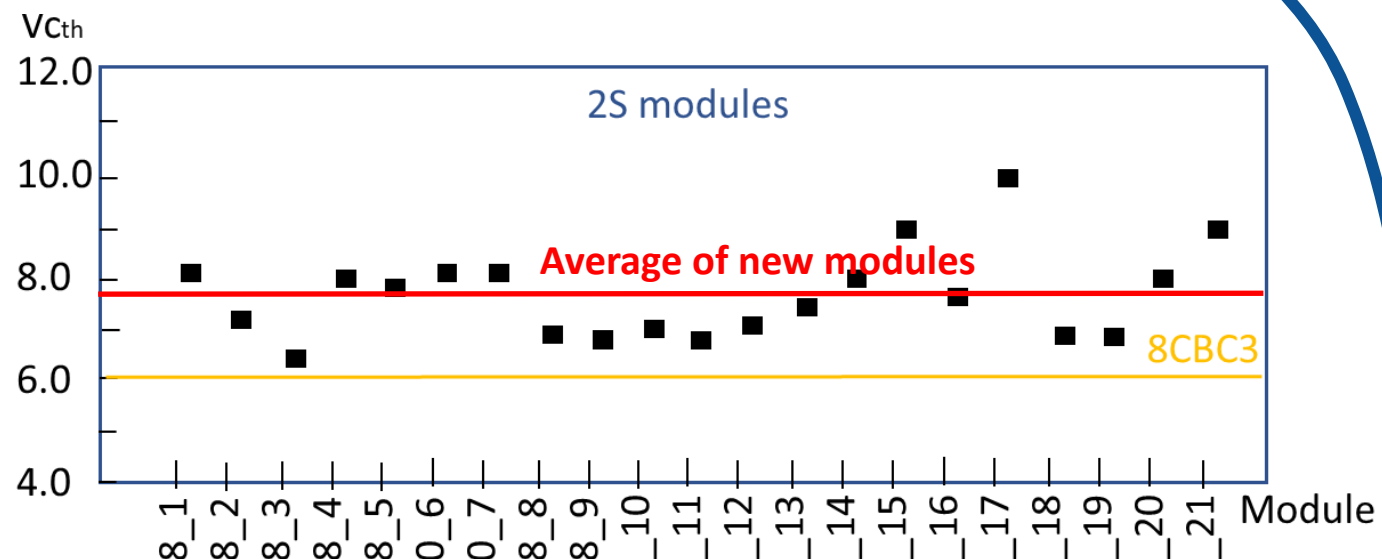*Figure 4: Noise measurements from PS prototype modules.*

Figure 5: Noise measurements from 2S prototype modules.

3. The Investigation

Debugging a noise sensitive, complex system:

- **Explorative measurements** with near field probes and oscilloscopes. **Searching for correlations** between noise and usage of different grounding schemes, disconnection of certain elements like sensors, cables and circuits (figures 6, 7, 8).

- **Building models** of noise injection that can explain any findings from the above investigation (figure 9).

- **Testing the models** formed by checking their predictive power (figures 9, 10).
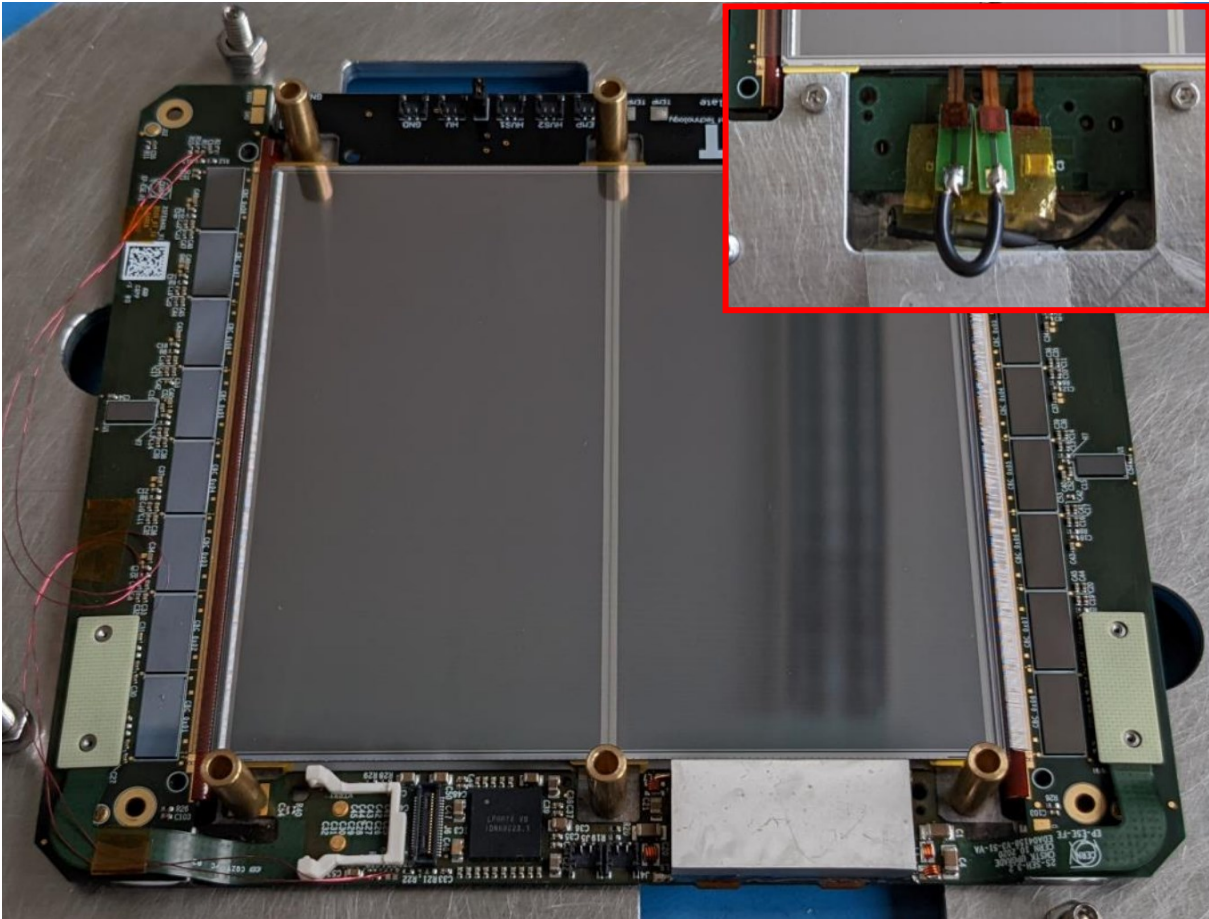

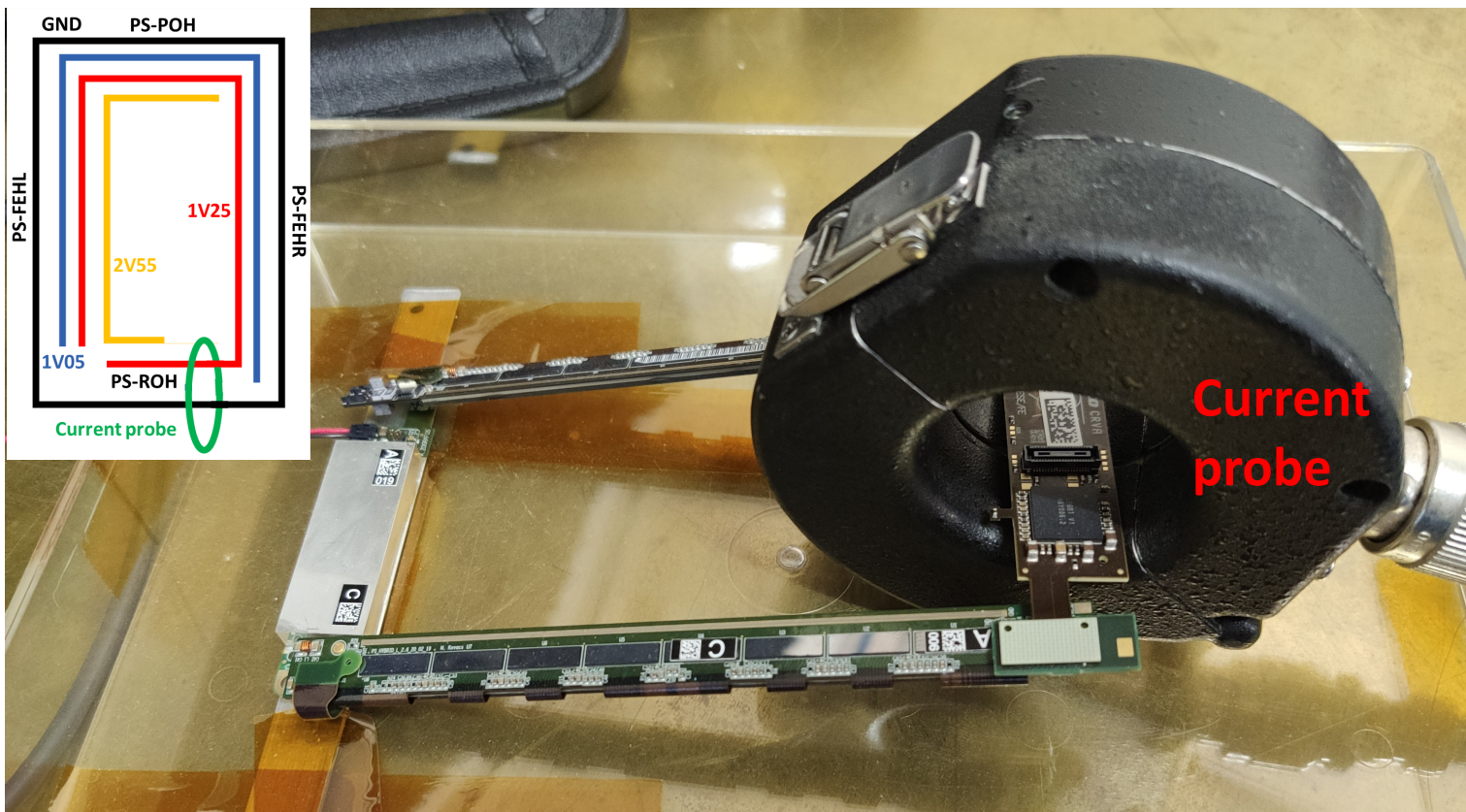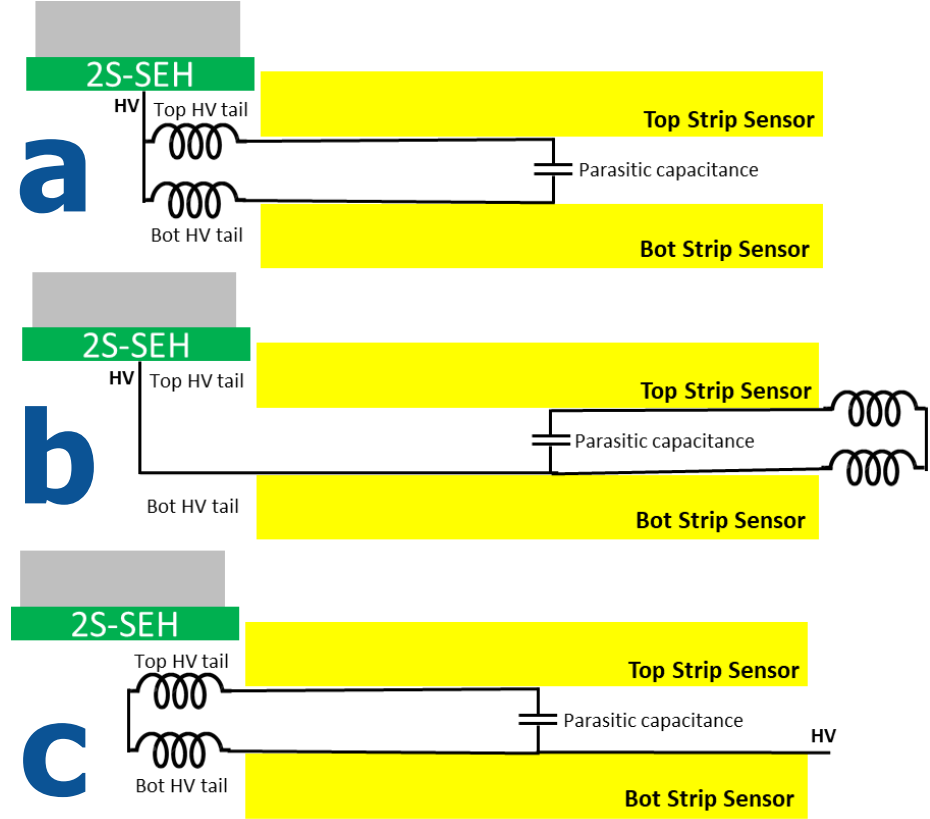*Figure 6: 2S module "Frankenstein", used to perform dozens of tests.*

Figure 7: Current probe connected to an EMI receiver used to perform measurements on a PS skeleton. Only GND net is closing the loop allowing for indirect measurements on common mode GND noise.

Figure 8: Common mode currents detected with the setup of figure 7 presented in dBµA. Multiple frequencies visible from the operation of the DC-DC converters.

Figure 9: Different HV supplying schemes, "Frankenstein" module while testing the hypothesis of LC resonance with the HV tails.
a. Baseline —> high noise
b. Same LC —> low noise
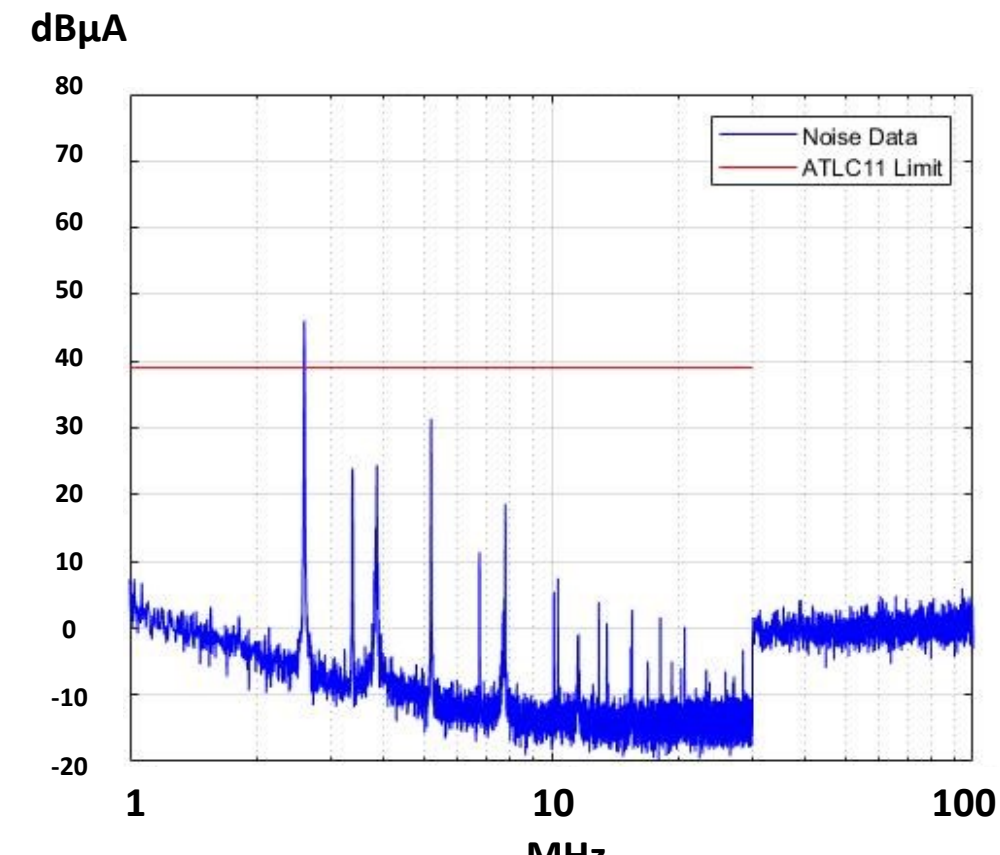*c. Same LC no connection to 2S-SEH with HV tails —> high noise*
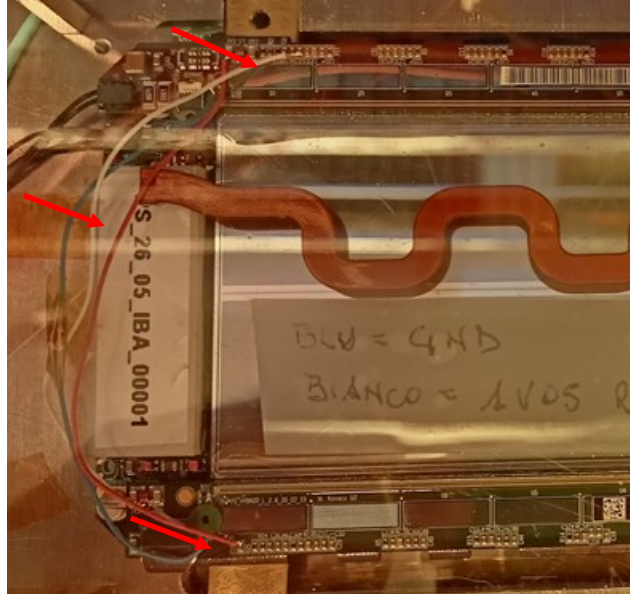
Figure 10: PS module with patches to change powering scheme.

4. Noise Conclusions

Two main **noise sources** were identified and proven to play the biggest role:

i) Switching currents from the operation of the DC-DC converters on the hybrids (switching @ 2.5 Mhz and 4 MHz) generate **common mode voltage on the GND**. This voltage generates currents that flow on the modules which injects noise indirectly to the analog front-ends but also affect them directly because of the voltage difference between the GND of the HV circuit and the GND of the analog front-end (figure 11). Both PS and 2S modules are affected by this.
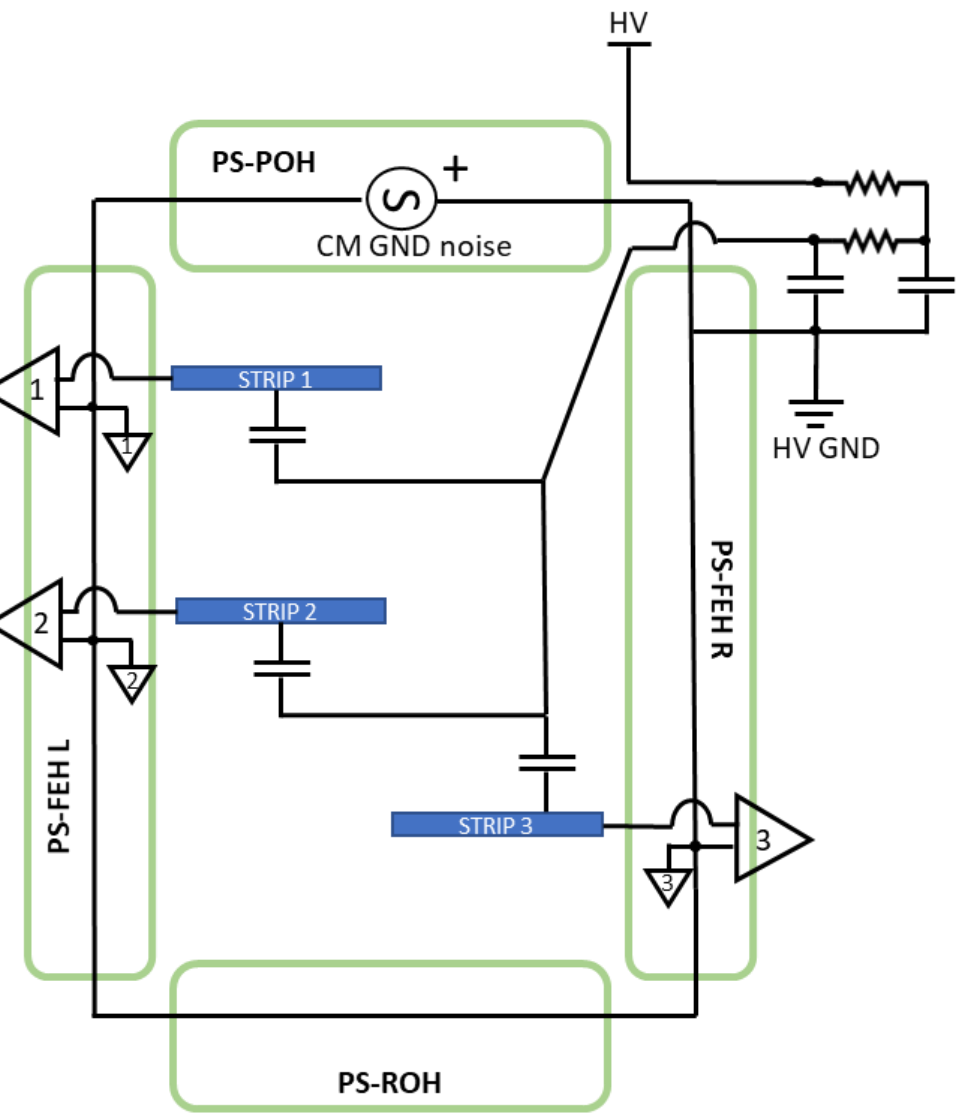
ii) **Time-varying magnetic field** is escaping through the PCB of the 2S-SEH and gets **picked-up by a small loop** formed by the two **HV tails** that are connecting underneath the 2S-SEH (figure 13). This loop at the frequencies relevant for the analog front-ends (>10 Mhz) has **small impedance** (~Ω). As a result, a very small electromotive force is capable of generating large noise currents which appear as noise in the analog front-ends. In the 2S module this effect was shown to create noise. In the PS case, a similar, low impedance loop exists as well and presents as a vulnerability to external noise.

Figure 11: GND diagram of a PS module. Similar to the 2S case.
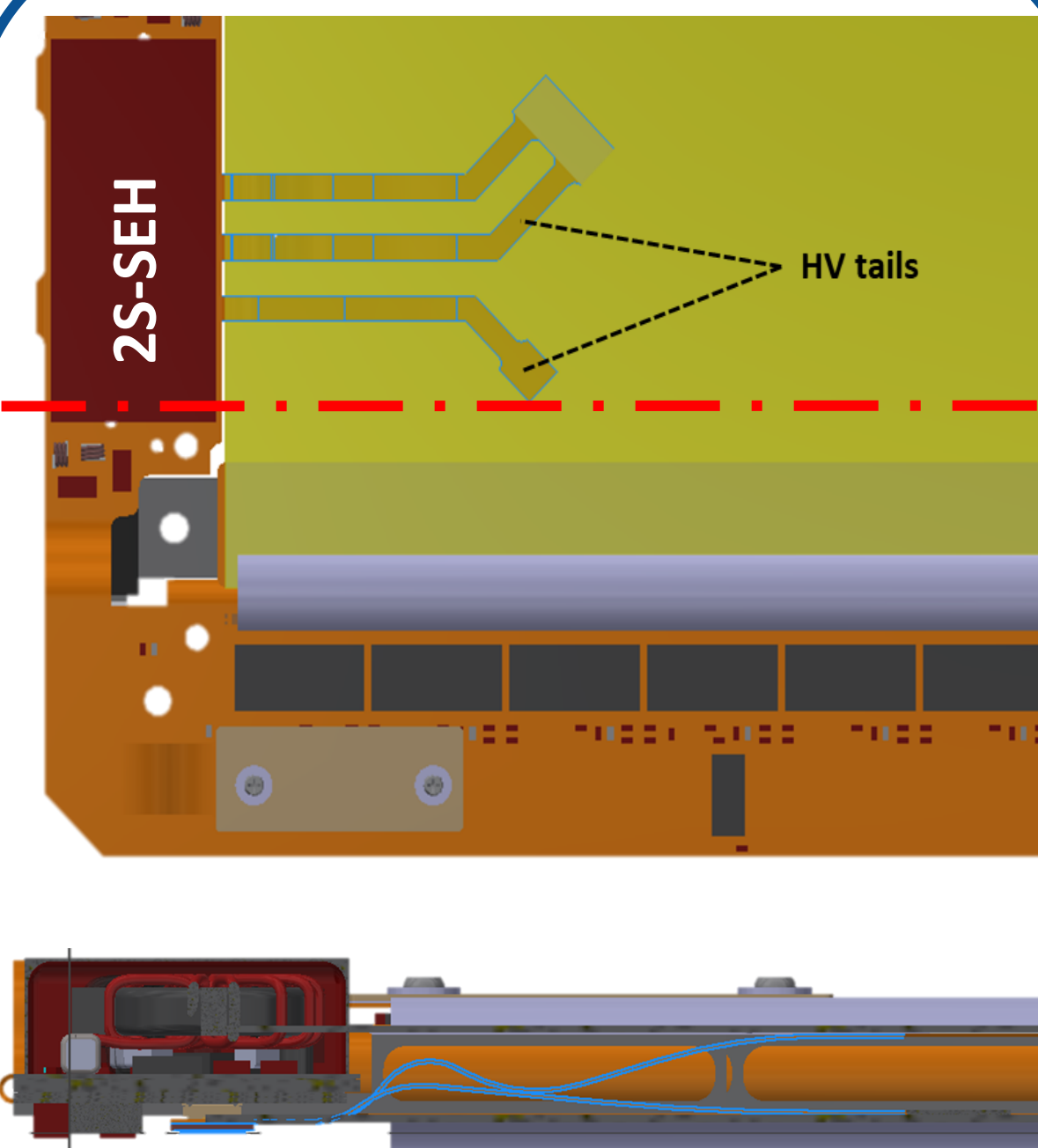

Figure 12: Top and side view (slice on red line) of the 2S module. Light blue marks the HV tails. Both HV tails connect to a single net underneath the 2S-SEH. In the side view the air-core coil of the 2S-SEH is also visible.
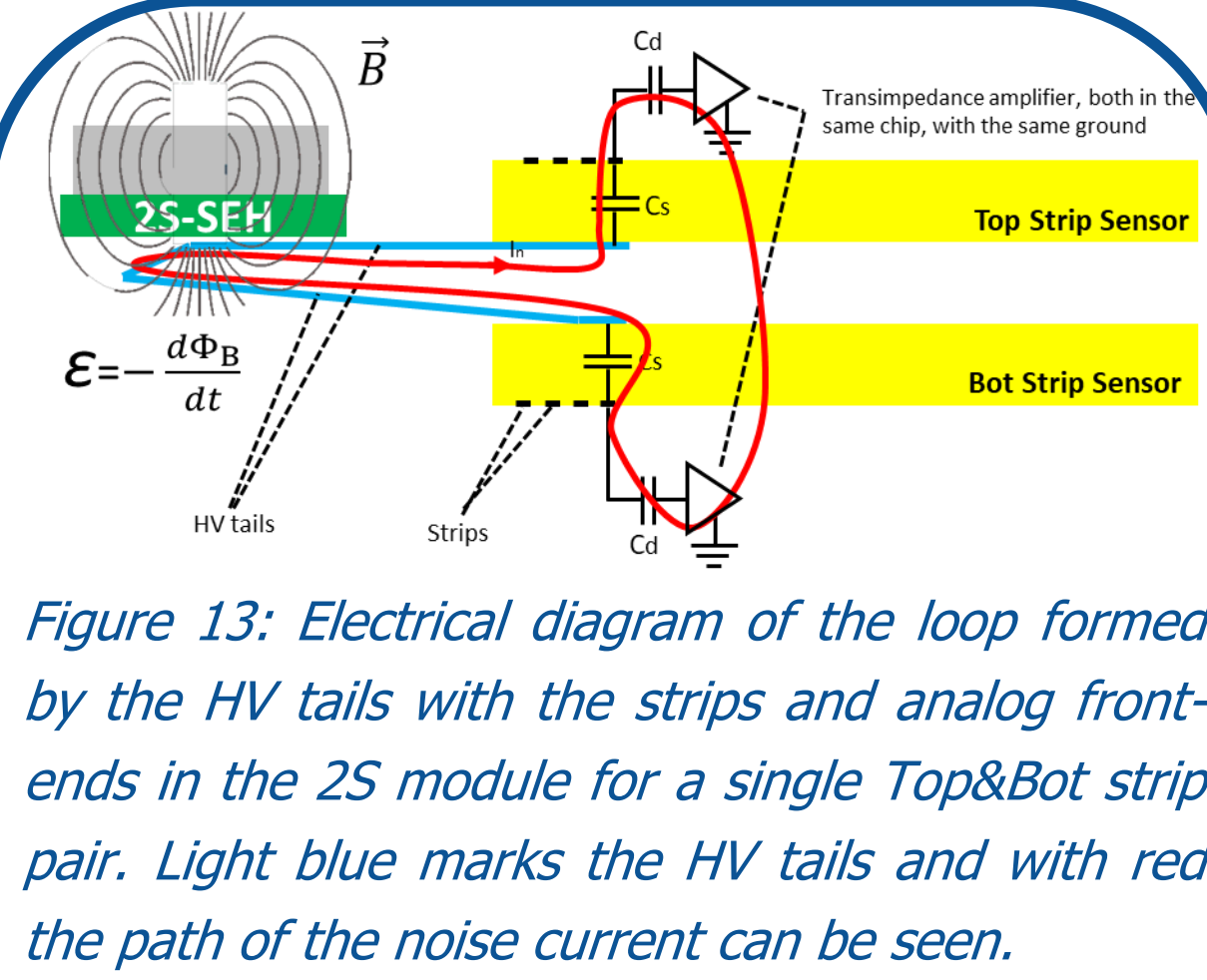

Figure 13: Electrical diagram of the loop formed by the HV tails with the strips and analog front-ends in the 2S module for a single Top&Bot strip pair. Light blue marks the HV tails and with red the path of the noise current can be seen.
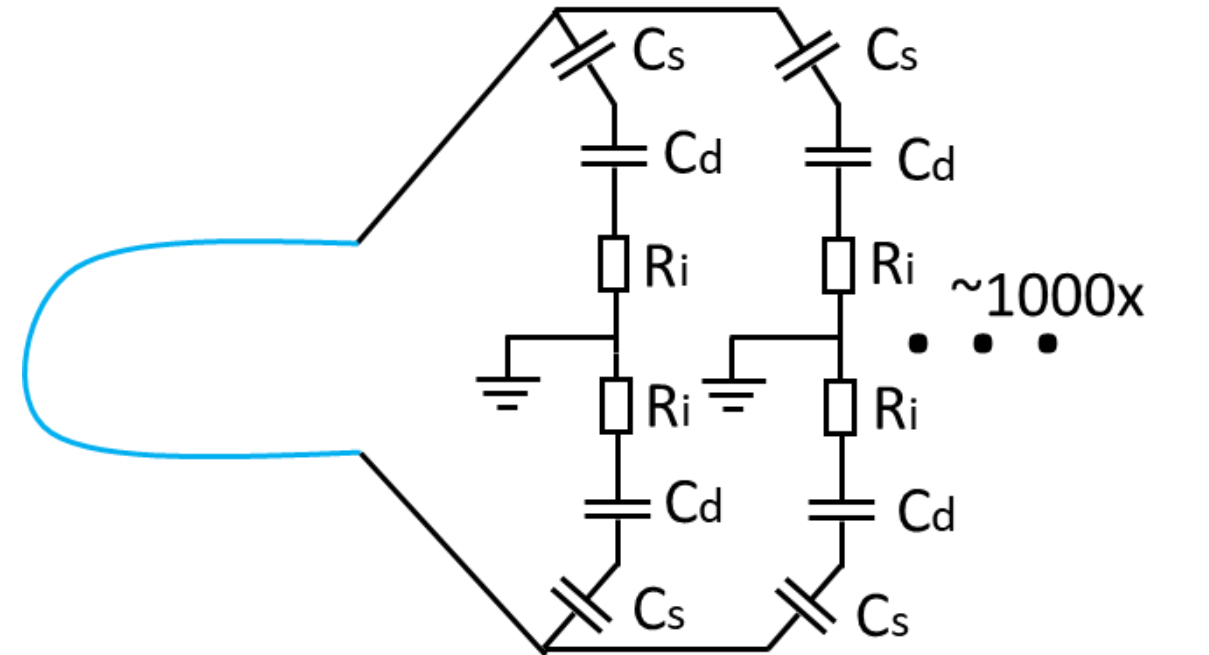
$$\mathcal{E} = -\frac{d\Phi_B}{dt}$$

Figure 14: Abstracted electrical diagram for the full 2S module strips and HV tails. Cs~10 pF, Cd~100 pF, Ri~ kΩ @ frequencies of interest.
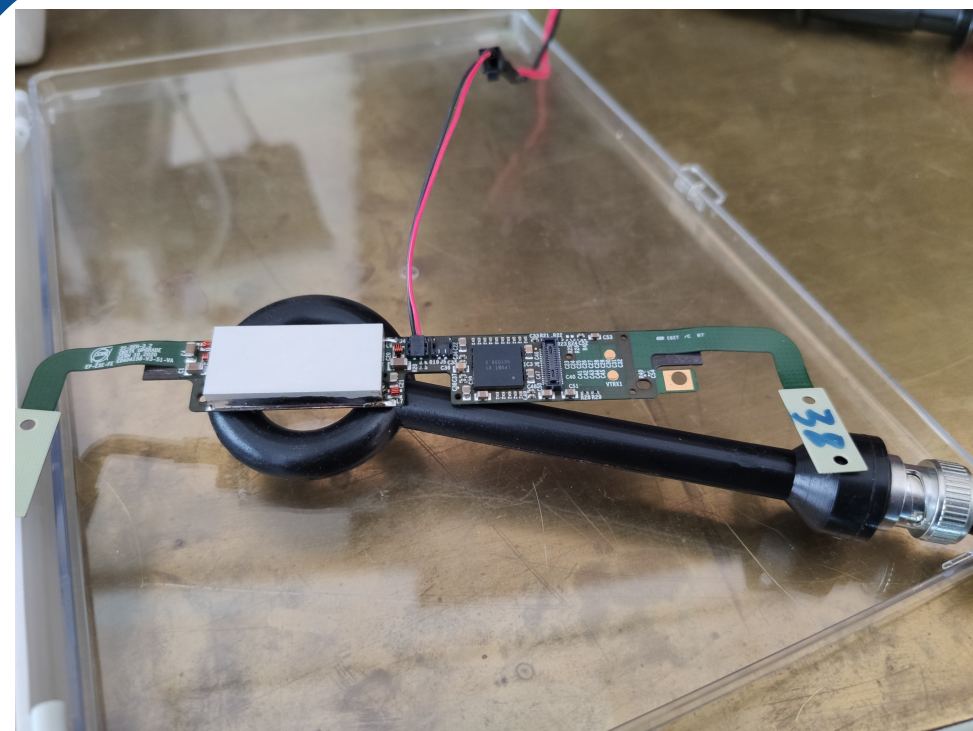

Figure 15: Near field 3 cm loop probe under the 2S-SEH.
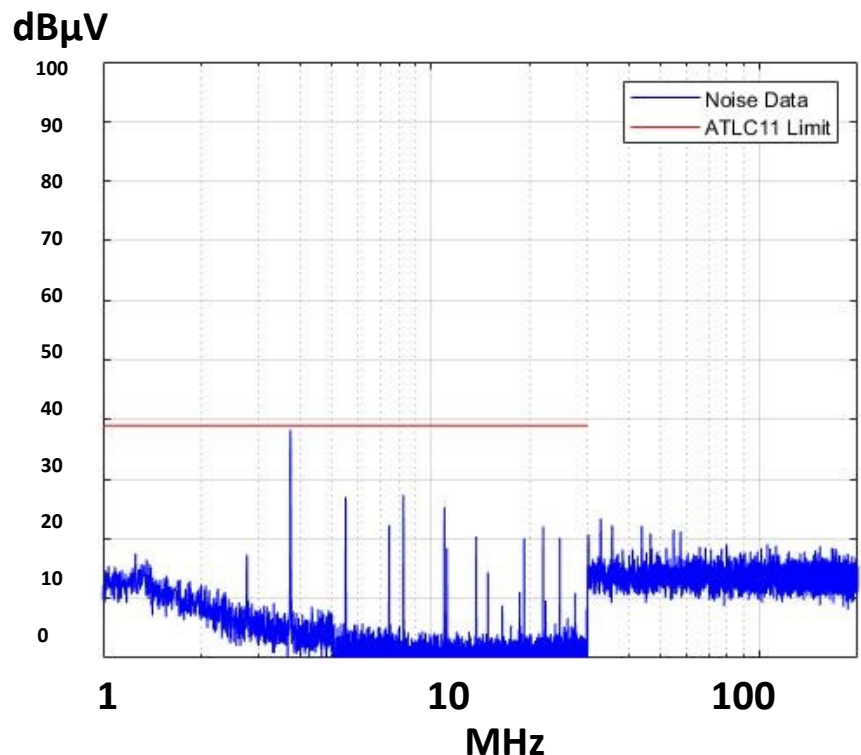

Figure 16: Measurements from setup of figure 15 in dBµV. Many high frequency components clearly visible.

5. Hybrid Changes

Main changes implemented for the production of the hybrids:

i) **Insertion of a small** (100 Ω) **resistor** in series with the loop of figure 14 in the 2S and PS modules. This changes the impedance of the loop by orders of magnitude, making it relatively impervious to magnetic fields.

ii) **Removal of output capacitor** in the HV filter of 2S and potentially PS (figure 17). This restricts the capability of the HV circuit and analog front-end GND difference to generate high noise currents.

iii) **PCB design change** to **separate the GND** on which the DC-DC converters operate in and the GND that is distributed to left and right side hybrids (figure 18) on PS and 2S.
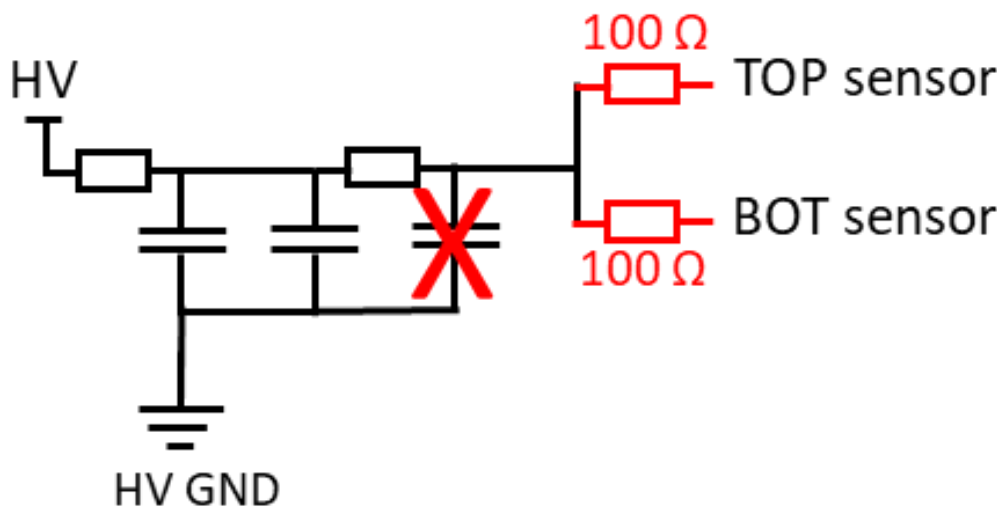
The **challenge** with **implementing** the **separated GND** plane design in both PS and 2S cases is clear:

- Unavoidable **increase in the resistance of the GND** in one of the two sides has to be **minimized**. In the PS-POH case the new design -after optimization- leads to 13 mV of GND drop (7.5 mV originally) on the left side at the nominal load and an 11% increase in PCB power losses (figure 19).

- **Considerations** have to be made for GND on the **output Pi filters** of the DC-DC converters in the new scheme. In the new scheme the CM voltage is "redirected" as small ripple on the 2V55 and 1V05 rails (figure 18).

- **Effect** of such a design has to be **studied in advance** as much as possible (figure 20).
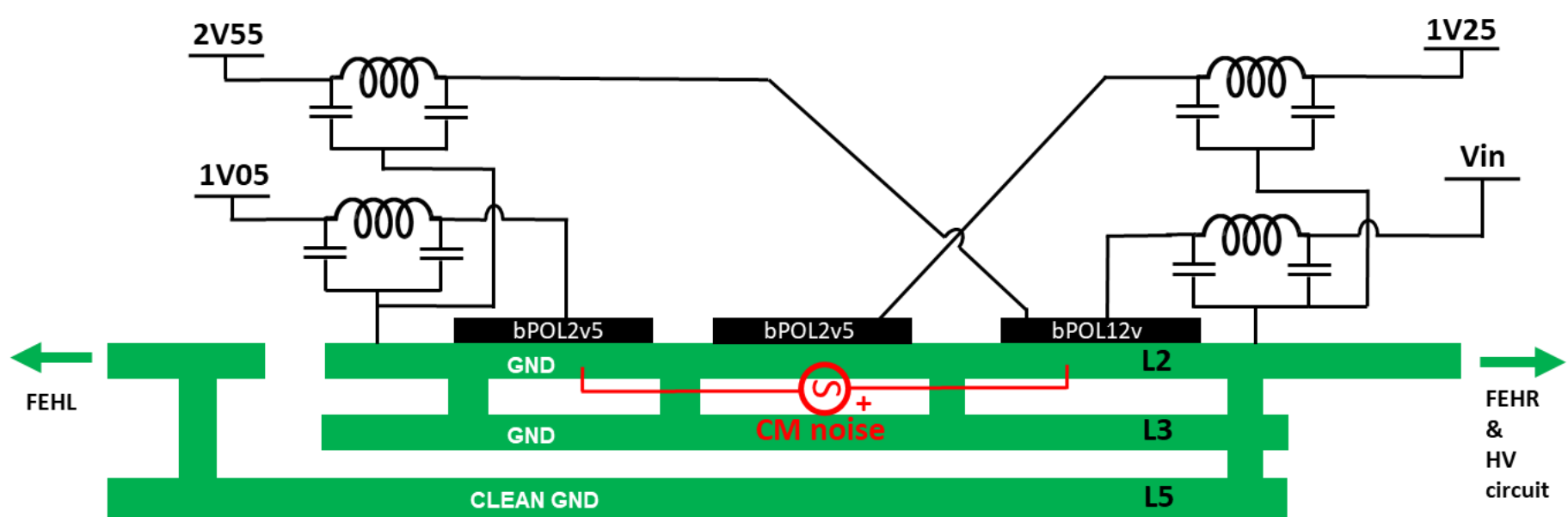

Figure 17: HV circuit changes.

Figure 18: Side view of GND planes of the PS-POH.
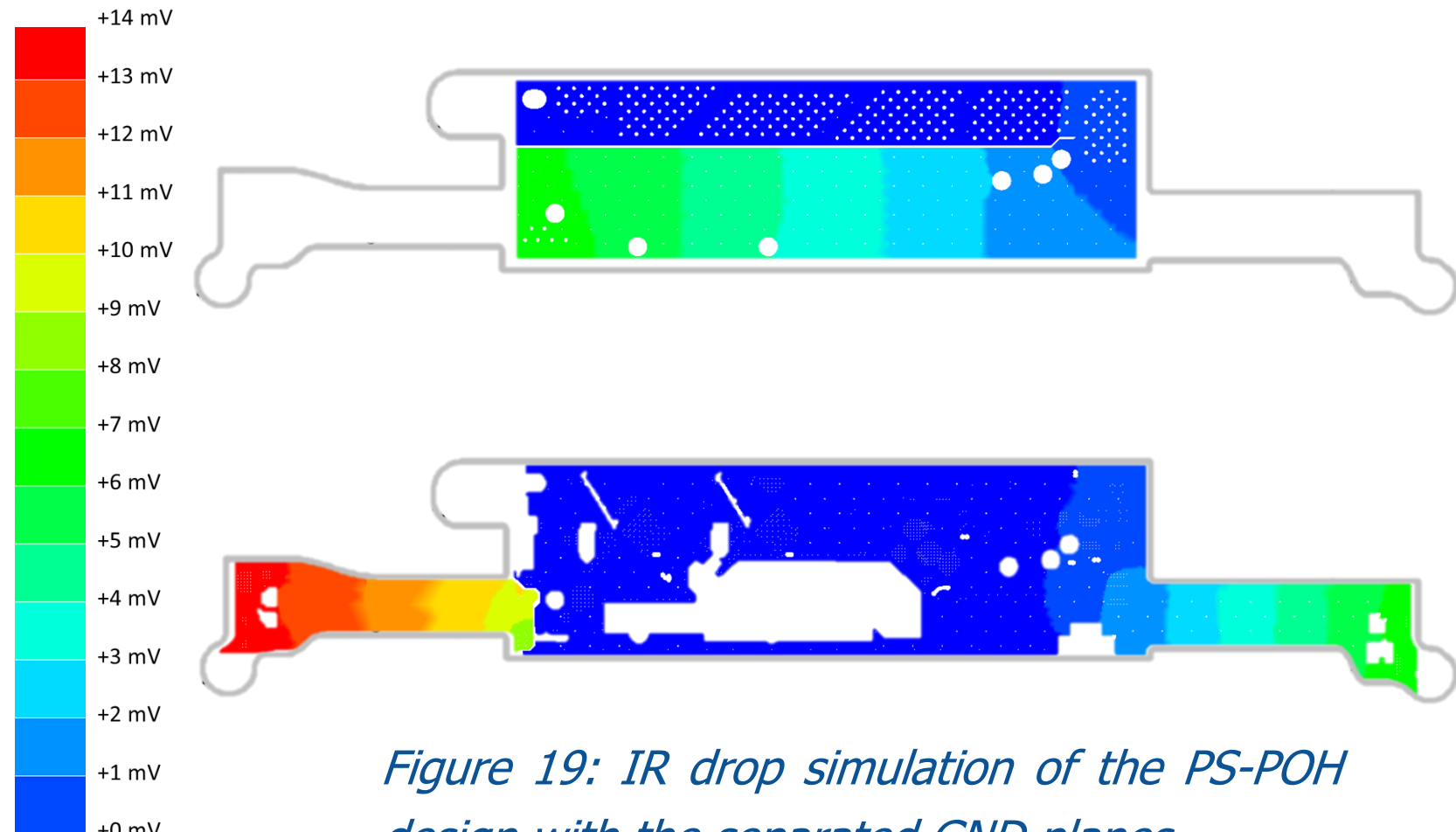
Figure 19: IR drop simulation of the PS-POH design with the separated GND planes.
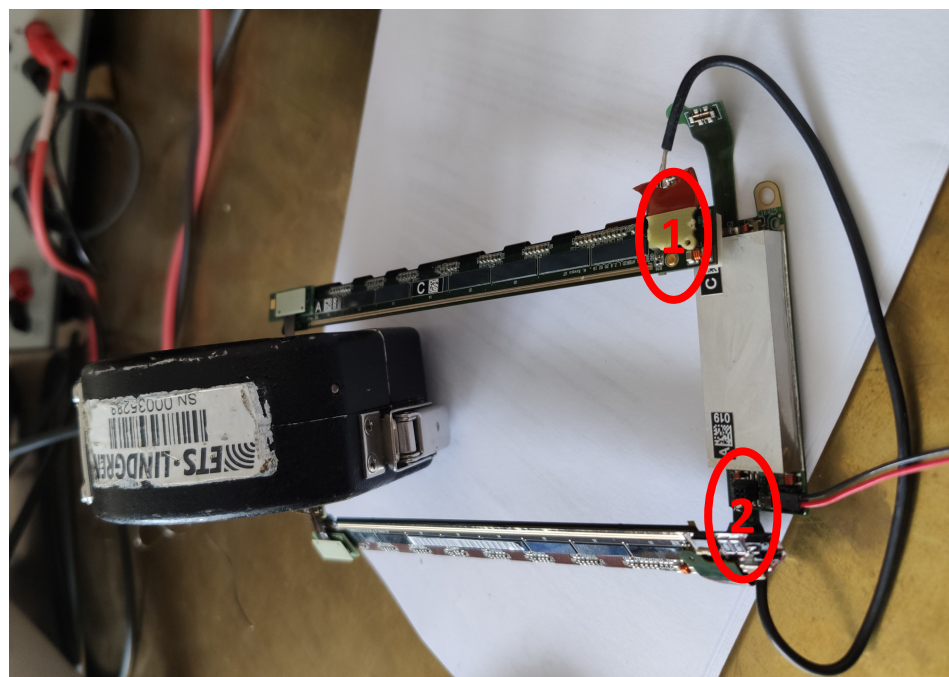

Figure 20: PS skeleton with similar setup to figure 6. GND connection to left side (marker 1) is now from a point on the PS-POH closer to the right side (marker 2).
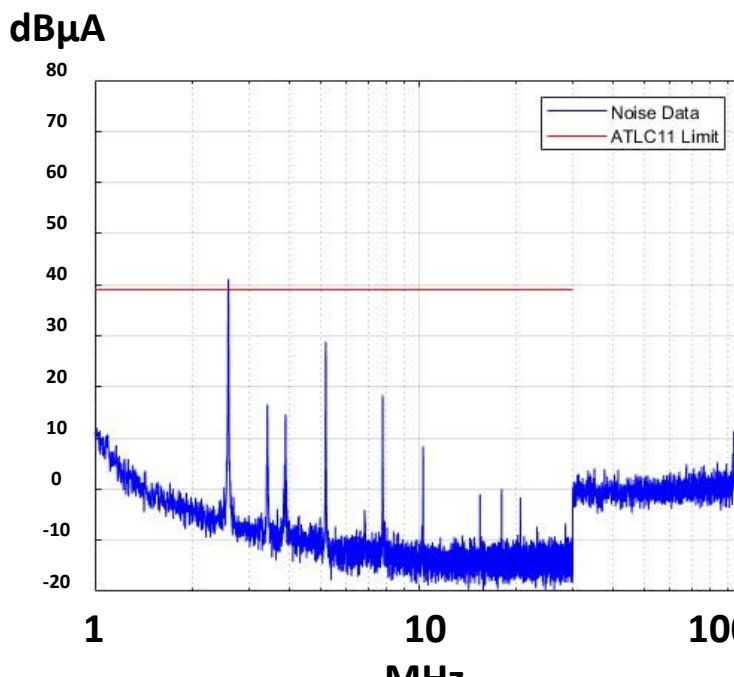

Figure 21: Common mode currents detected with the setup of figure 20. Significant improvement compared to figure 8.